IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Eliyahou Harari et al.		
Title:	Flash EEprom System		
Application No.:	09/114,504	Filing Date:	July 13, 1998
Examiner:	Vu Anh Le	Group Art Unit:	2824
Docket No.:	SNDK.006USQ	Conf. No.:	9326

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF UNDER 37 C.F.R. 41.37
ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

In response to the Notification of Non-Compliant Appeal Brief mailed on September 7, 2006, and Pursuant to 37 C.F.R. § 1.191 and the Notice of Appeal filed in this application on May 3, 2006, Applicants submit this revised Appeal Brief. A two-month extension of the reply period is request, thereby extending the reply period to December 7, 2006. The Summary of Claimed Subject Matter, Related Appeals and Interferences, and the Evidence and Related Proceedings Appendices have amended to conform to the remarks of the Notification. The Commissioner is authorized to deduct any amounts required for this Appeal Brief and to credit any amounts overpaid to Deposit Account No. 502664.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is SanDisk Corporation, a corporation of the state of Delaware, the assignee of all right, title and interest in the present patent application from the inventors, Eliyahou Harari, Robert D. Norman, and Sanjay Mehrotra.

II. RELATED APPEALS AND INTERFERENCES

Several applications that share disclosure with the present application, all similarly claiming priority from, and limited to the matter disclosed in, US patent application number 07/337,566, have been involved in an appeal, interference, or judicial proceeding. Although they may not have a direct bearing on the present appeal, the following list is provided here through an abundance of caution:

US patent application number 09/103,056 has been involved in Patent Interference No. 104,760. The decision from this Interference is included in the Related Proceedings Appendix.

US patent application number 09/056,398 has been involved in an Appeal. The decision from this Appeal is included in the Related Proceedings Appendix.

A Notice of Appeal and Appeal brief were filed in US patent application number 10/417,954, but the appeal did not go forward and the examiner reopened prosecution. Consequently, there is no decision and the inclusion of one is *not applicable.*

An appeal is currently pending in US patent application number 10/000,155. Consequently, there is as yet no decision and the inclusion of one is *not applicable.*

US patent number 5,418,752 has been involved in a U.S. International Trade Commission action, Investigation No. 337-TA-382. The decision from this action is included in the Related Proceedings Appendix.

US patent number 5,602,987 has been involved in litigation, *SanDisk Corporation v. Lexar Media, Inc.*, United States District Court for Northern California, San Francisco Division, Case No. C98-0111 CRB (PJH). This case was settled. Consequently, there is no decision and the inclusion of one is *not applicable.*

US patent number 5,602,987 is involved in pending litigation. The decision from an appeal in this case, *SanDisk Corporation v. Memorex Products, Inc.*, 415 F.3d 1278, 75USPQ 2D1475 (Fed. Cir. 2005), is included in the Related Proceedings Appendix.

US patent number 5,719,808 is involved in pending litigation, *STMicroelctronics, Inc. v. SanDisk Corporation v. STMicroelctronics, Inc.,* United States District Court for the Eastern District of Texas, Sherman Division, Case Action No. 4:05CV45. Consequently, there is as yet no decision and the inclusion of one is *not applicable.*

III. STATUS OF THE CLAIMS

The subject application was filed July 13, 1998, and is a continuation of patent application serial no. 08/931,133, filed September 16, 1997, now patent no. 5,936971, which is a continuation of patent application serial no. 08/249,049, filed May 25, 1994, now patent no. 5,671,229, which is a continuation of patent application serial no. 07/963,837, filed October 20, 1992,now abandoned, which in turn is a division of patent application serial no. 07/337,566, filed April 13, 1989, abandoned. The original parent application claims 1-62 were cancelled in a Preliminary Amendment filed concurrently with the subject application on July 13, 1998. This Preliminary Amendment also added claim 63, which was a substantial copy of claim 1 of U.S. patent no. 5,648,929 - Miyamoto - granted July 15, 1997.

In the first Office Action on the merits (mailed September 28, 1998), claim 63 was allowed. A Continued Prosecution Application filed on December 28, 1998, amended claim 63 to clarify the scope of the present application and added claims 64 and 65. An Office Communication (mailed March 26, 1999) suspended prosecution due to questions of interference. The next subsequent communication was an Office Action (mailed February 14, 2003) that rejected claims 63-65 under 35 U.S.C.112, first paragraph, for the written description requirement, in response to which an Amendment (May 1, 2003) was filed that modified the claims ("logic blocks" was changed to "blocks"). The next (non-final) Office Action (mailed on December 3, 2004) rejected claims 63-65 on new grounds under 35 U.S.C.112, first paragraph, as failing to comply with the enablement requirement due to the "data control logic circuit" and "an address control logic circuit" elements of the claims. A Response (mailed March 2, 2005) argued that the 35 U.S.C. 112, first paragraph, rejection was not well founded and that the

enablement requirement was met. The subsequent, and most recent, non-final Office Action (mailed on October 25, 2005) again rejected claims 63-65 under 35 U.S.C.112, first paragraph, as failing to comply with the enablement requirement due to the "data control logic circuit" and "an address control logic circuit" elements of the claims, but the details of the rejection differ from those given in the preceding Office Action.

Claims 63-65 stand rejected under 35 U.S.C. §112, first paragraph, as the Applicants allegedly failed to comply with the enablement requirement with respect to the elements of "a data control logic circuit ..." and "an address control logic circuit ...".

Claims 1-62 have been cancelled.

IV. STATUS OF AMENDMENTS

On March 27, 2006, a Notice of Appeal from the Examiner's decision rejecting claims 63-65 was filed. No Amendments have been filed since the October 25, 2005, mailing date of the Office Action from which this Appeal is being taken.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As background, this section gives a summary of the present invention. Since the claims stand rejected under the written description requirement of 35 U.S.C. §112, first paragraph, some of this material is presented in more detail below in section VII in order to demonstrate that the specification of the subject application is enabling.

The claimed subject matter is a flash memory card whose memory has multiple partitions, with each partition divided into multiple physical blocks. The card includes a connector, for attaching to an external device; data control logic circuitry, for controlling the transfer of data through the connector between the card's memory and external to the card; and address control logic circuitry to assign corresponding physical addresses in the memory blocks to addresses received via the connector. When erase commands for multiple memory blocks are input via the connector, the data control logic circuitry transmits these to the blocks to be erased and the address control logic circuitry transmits chip enable signals to at least two of the memory partitions to be erased so that at least two of partitions are busy at the same time, allowing any combination of sector blocks to be erased together.

The pending independent claims are claims 63, 64, and 65. In claim 63, the flash memory card is presented as:

> 63. A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, comprising:
>
> a connector for connecting said flash memory card to an external device;
>
> a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and
>
> an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

Claim 64 is explicitly for the case where multi-state memory cells are used:

> 64. A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, each of the physical blocks having a plurality of flash memory cells, each flash memory cell being individually programmable into more than two states in order to store more than one bit of data per cell, comprising:
>
> a connector for connecting said flash memory card to an external device;
>
> a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and
>
> an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

And claim 65 is explicitly for the case where binary memory cells are used:

> 65. A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, each of the physical

blocks having a plurality of flash memory cells, each flash memory cell being individually programmable into two states in order to store one bit of data per cell, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

In the application, such flash memory cards are described generally between page 6, line 1, and page 8, line 5, with respect to Figures 1A and 1B. Figure 1A shows a flash memory device 29 having a controller 31 and a memory array 33. In Figure 1B, the array 33 is shown to be partitioned into a number of chips (43, 54, ..., 47) with the corresponding chip select signals noted at 49, 51, ..., 53. Erase operations are described primarily in the "Erase of Memory Structures" section at page 8, line 6, to page 14, line 11, with respect to Figures 2, 3A, 3B, and 4. Figure 2 shows the division of memory partitions (chips) into sector blocks, with the hatching indicating sectors to be erased together. As also shown in Figure 2, line 209 connects the controller to the memory chips. As shown in Figure 3A and the detail in Figure 3B, the chips have control circuitry 225 and 229 that supplies received commands (global erase 251, set/clear erase 237, reset 261) from the controller to each sector's register 221. The chips have address circuitry 231 and 235 that supplies along 235 the received addresses from the controller to each sector's register 221. The enable erase command 251 from the controller is ANDed with the erase voltage from the controller and supplied to each sector. Various elements of the controller are shown in more detail in Figures 6, 7, and 8 and included various elements of data control logic (e.g., command sequencer 511) and address control logic (e.g., address generator 503). The assignment of received addresses to physical memory sector blocks in described, for

example, at page 17, line 26, to page 19, line 10, with respect to Figure 6 in the context of a read operation.

As described with respect to Figures 2-4 between line 10 of page 9 and line 11 of page 14, the sectors to be erased are determined by the control logic based upon the set erase enable commands 237 and addresses 235 from the controller as these are supplied to each sector block's register 221, along with the chip select signals 49, 51, ..., 53. When the global erase command 251 is asserted, at least two of the chips into which the memory is partitioned can then be erased at the same time, as shown with respect to Figure 2.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Board is asked to review the correctness of the rejections under 35 U.S.C. §112, first paragraph. Specifically, claims 63-65 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement with respect to both the "data control logic circuit" and the "address control logic" elements of the claims. The Office Action alleges that the specification is not enabling with respect to four points:

i) "The data control logic circuit and the address control circuit are two separate circuits while the specification shows only one controller ... for controlling flash EEPROM array";

ii) "The controller ... can not be considered as **a data control logic circuit** since the controller ... does not '***transmitting block erase commands*** to the flash memory partitions including the physical blocks ***to be erased*** when the block erase commands associated with a plurality of blocks are inputted via said connector'"[emphasis in Office Action];

iii) "The controller ... can not be considered as 'an address control logic circuit for managing addresses ... by ***assigning*** *the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions*'"[emphasis in Office Action];

iv) "the controller .. can not be considered as the address control logic circuit since the controller ... does not 'transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased'".

These are the bases for rejecting all of the claims and are the sole issues in this appeal.

All of the claims stand rejected under the same grounds and can be taken to form a single group, with independent claim 63 suitable for deciding whether this group of claims patentable.

VII. ARGUMENT

The most recent Office Action, from which this Appeal originates, rejects all of the pending claims under 35 U.S.C. §112, first paragraph, for failing to comply with the enablement requirement for several different reasons, as described in the preceding section. All of these claims are rejected on the same grounds, with all of the claims are argued together and, when reference to a specific claim is required, claim 63 is believed suitable for this purpose. Each of the different points noted in the last section will be treated under the corresponding sub-heading below. In each case, it is believed that the cited description is enabling.

i) "two separate circuits while the specification shows only one controller"

The Office Action states:

> The data control logic circuit and the address control circuit are two separate circuits while the specification shows only one controller 31 (Fig. 1) for controlling flash EEPROM array33.

This is believed to be both an incorrect and an improper basis for a rejection.

First, there appears to be no basis for this particular objection in terms the claims themselves: the claims include "a data control logic circuit" and "an address control logic circuit", but there is nothing in the claim whereby these elements cannot both be within the same controller. Further, based on the language of the claims, there is nothing to prevent these circuits from sharing some, or even all, of their elements. The Office Action appears to either be improperly interpreting the claim, improperly importing limitations into the claims, or both.

Secondly, regardless of the lack of basis for this objection, it is noted that exemplary embodiments of the controller of the present application include distinct control and address elements that perform the various limitations recited in the claims as discussed in the following points. More detail of controller of the present application are described in more detail with respect to Figures 6 and 7. As shown there, the controller 31 includes logic circuitry specific to both data control functions (e.g., command sequencer 511, DMA controller 507) and address

control functions (e.g., address generator 503, comparator 509). These various controller elements are described at length beginning at page17, line 26. (The various limitations of these logic circuits for which the Office Action alleges a lack of enablement are discussed further below under the corresponding headings: The present section is only related to the Office Action's rejection based on these elements both being part of the controller.)

Based on these comments quoted at the beginning of this subsection, the Office Action seems to be requiring that present application provide not just support for the claims as written, but for a specific embodiment–or, perhaps more accurately, seems to require support for ruling out a particular embodiment. This is improper. The correct question is whether the present specification is enabling for the claims ***as written***. The claims contain ***no such limiting language*** (such as "wherein said data control logic circuit and address control circuit are not part of a single controller" or other such limiting language) that would restrict that would restrict them in this way. As noted in 37 CFR 41.200(b), "[a] claim shall be given it broadest reasonable construction. …". Similarly, as noted in the M.P.E.P.§2111, claims must be given their broadest reasonable interpretation; in contrast, the Office Action appears to be reading limitations into the claim that are not there and then improperly issuing a rejection on this basis. As noted above, support for the disputed claim element *as written* is explicitly given in Figures 6 and 7 and their corresponding description beginning at page17, line 26.

(As noted above in Section III above, the currently pending claim 63 in the present application is a substantial copy of claim 1 of U.S. patent no. 5,648,929. Although not explicitly stated in the Office Actions, it may be that the Office Action is requiring that the present application provide not just support for the claims as written, but for a specific embodiment of U.S. patent 5,648,929. This is again improper and the correct question is whether the present specification is enabling for the claim ***as written***.)

ii) "controller … does not '***transmitting block erase commands***'"

The Office Action states:

> The controller 31 can not be considered as **a data control logic circuit** since the controller 31 does not "***transmitting block erase commands*** to the flash memory partitions including the physical blocks ***to be erased*** when the block erase commands associated with a plurality of blocks are inputted via said connector". The specification teaches "the controller then issues to the circuit 220, as well as all other chips in the

> system a global erase command in line 251 alone with the high voltage for erasing in line 209" (page 10, lines 33-35 and page 11, line 1). It means that the controller **issues** a **global** erase command (not ***transmitting a block*** erase command) to all other chips in the system (not to only the flash memory partitions including the physical blocks to be erased). [emphasis in Office Action]

It is believed that not only is the present application enable for the cited limitation, but that the Office Action is also reading limitations into the claim, improperly interpreting the claim, or both. In addition the global erase command noted above, the applications also includes set "erase enable" signals.

First, in addition to the global erase command (in line 251, Figure 3A), the present application also introduces a "set erase enable command". As shown in Figures 3A and 3B, the set erase enable command is supplied along line 237 to the registers 221 associated with each of the sector blocks (211, 213) that are to be erased. This erase enable command is provided to the registers 221 from the command decoder 229 and register 225 circuitry, where they are placed after being received at the chip from the control circuitry of the controller. This is described in the application beginning at page 9, line 30:

> Figure 3A illustrates a block diagram circuit 220 on a Flash EEprom chip (such as the chip 201 of figure 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase. Essentially, each sector such as 211, 213 is selected or tagged by setting the state of an erase enable register such as 221, 223 associated with the respective sectors. The selection and subsequent erase operations are performed under the control of the controller 31 (see figure 2). The circuit 220 is in communication with the controller 31 through lines 209. Command information from the controller is captured in the circuit 220 by a command register 225 through a serial interface 227. It is then decoded by a command decoder 229 which outputs various control signals. Similarly, address information is captured by an address register 231 and is decoded by an address decoder 233.
>
> For example, in order to select the sector 211 for erase, the controller sends the address of the sector 211 to the circuit 220. The address is decoded in line 235 and is used in combination with a set erase enable signal in bus 237 to set an output 239 of the register 221 to HIGH. This enables the sector 211 in a subsequent erase operation. Similarly, if the sector 213 is also desired to be erased, its associated register 223 may be set HIGH.
>
> Figure 3B shows the structure of the register such as 221, 223 in more detail ...

It is respectfully submitted that the "erase enable" commands correspond to the "block erase commands" of the claim and that the specification is enabling with respect to controller, specifically its data control circuitry, transmitting such commands as presented in the claims.

Further, in the remarks quoted above, the Office Action states: "It means that the controller **issues** a **global** erase command (not ***transmitting a block*** erase command) to all other chips in the system (not to only the flash memory partitions including the physical blocks to be

erased)"; that is, it appears the Office Action appears to interpret the claim to mean that "block erase commands" of the claim should be sent *only* to the memory partitions having blocks to be erased. This is incorrect. More specifically, the relevant portion of the claim is

> a data control logic circuit ... respectively transmitting block erase commands *to the flash memory partitions including the physical blocks* to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector;

where the emphasis is added. Note the claim does not say *only* to those flash memory partitions having the physical blocks to be erased, but "to the flash memory partitions *including* the physical blocks to be erased". Consequently, the claims only requires that the "block erase commands" be sent to *at least* those memory partitions with sectors to be erased, not *only* to those memory partitions with sectors to be erased. It is unclear whether the Office Action is misinterpreting the claim or is again be improperly importing limitations from the patent from which claims have been taken and improperly asking for support of a particular embodiment. As discussed in the preceding section above, rather than of the claim *as written*.

iii) "controller can not be considered as 'an address control logic circuit for managing addresses ... by ***assigning*** *the addresses'"*

The Office Action states:

> The controller 31 can not be considered as "an address control logic circuit for managing addresses ... by ***assigning*** *the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions*" since the controller 31 does not managing addresses for the plurality of blocks by assigning the addresses to their corresponding addresses to their physical blocks". The specification only teaches "*the controller* ***sends*** *the addresses of the sector 211 to the circuit 220*" (page 10, lines 13-14). [emphasis in Office Action]

The Office Action is correct in that the cited location (page 10, line 13-14), and more generally at page 9, line 30, to page 11, line 6, describes the sector addresses being sent by the controller and received at the memory chips, rather than an assignment; however, the "assignment" is presented in other portions of the application.

More specifically, the relevant portion of the claim is

> an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions

Details of this sort of managing of the input addresses so that they are dispersed into the physical sector blocks on the chips is presented in a number of locations in the application. For example, in the context of the read operation, this is described beginning at page 17, line 26:

> Figure 6 illustrates the read data path control in the preferred embodiment. A memory device 33 which may include a plurality of Flash EEprom chips is under the control of the controller 31. The controller 31 is itself part of a microcomputer system under the control of a microprocessor (not shown). To initiate the reading of a sector, the microprocessor loads a memory address generator 503 in the controller with a memory address for starting the read operation. This information is loaded through a microprocessor interface port 505. Then the microprocessor loads a DMA controller 507 with the starting location in buffer memory or bus address that the data read should be sent. Then the microprocessor loads the header information (Head, Cylinder and sector) into a holding register file 509. Finally, the microprocessor loads a command sequencer 511 with a read command before passing control to the controller 31.
>
> After assuming control, the controller 31 first addresses the header of the sector and verifies that the memory is accessed at the address that the user had specified. This is achieved by the following sequence. The controller selects a memory chip (chip select) among the memory device 33 and shifts the address for the header area from the address generator 503 out to the selected memory chip in the memory device 33. The controller then switches the multiplexer 513 and shifts also the read command out to the memory device 33. Then the memory device reads the address sent it and begins sending serial data from the addressed sector back to the controller. A receiver 515 in the controller receives this data and puts it in parallel format. In one embodiment, once a byte (8 bits) is compiled, the controller compares the received data against the header data previously stored by the microprocessor in the holding register file 509. If the compare is correct, the proper location is verified and the sequence continues.

This passage describes how an input address, such as in the from of head, cylinder and sector, is assigned to corresponding physical sector blocks and memory chips of the memory. Consequently, it is believed that the application, both in the quoted portion and elsewhere, is more than adequate to meet the enablement requirement with respect to this limitation.

iv) "controller … does not 'transmitting chip enable signals'"

The Office Action states:

> Further, the controller 31 can not be considered as the address control logic circuit since the controller 31 does not "transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased".

This is also believed to be incorrect and it is respectfully submitted that the application complies with the enablement requirement.

Figure 1B shows the array 33 is shown to be partitioned into a number of chips (43, 54, …, 47) with the corresponding chip select and enable lines indicated at 49, 51, …, 53, as noted at

page 7, lines 14-16. The use of these chip enable signals by the controller in the addressing process is described, for example (again in the context of the read process), beginning at line 10 of page 18:

> After assuming control, the controller 31 first addresses the header of the sector and verifies that the memory is accessed at the address that the user had specified. This is achieved by the following sequence. The controller selects a memory chip (chip select) among the memory device 33 and shifts the address ...

The application also presents an erase specific enable signal for the chips, the "global erase command" in line 251 of Figure 3A. As described at page 10, line 32, to page 11, line6, this signal is transmitted from the controller to all the chips in the system, including those where erase operations are to be performed, as part of the addressing process. As shown at the bottom Figure 3A, after ANDing with the erase voltage on line 209 this enable command on line 251 is and supplied to each of the sectors "at least two of the plurality of flash memory partitions including the physical blocks to be erased".

Thus, it is believed that application is enabling for this limitation for both the chip select and enable lines indicated at 49, 51, ..., 53 of Figure 2 and the global erase command in line 251 of Figure 3A.

VIII. CONCLUSION

It is Applicants' position, as indicated above, that the assertions of the Office Action are incorrect. In each of the cases described above, it is believed that disclosure provided by the subject application meets the enablement requirements. Accordingly, the rejection of the application should be reversed and the present patent application passed to issue.

Respectfully submitted,

12/5/06

James S. Hsue
Reg. No 29,545

Date

PARSONS HSUE & DE RUNTZ LLP
595 Market Street, Suite 1900
San Francisco, CA 94105
(415) 318-1160 (main)
(415) 318-1162 (direct)
(415) 693-0194 (fax)

Appendix A

CLAIMS PENDING IN APPLICATION SERIAL NO. 09/114,504

Claims 1-62 are cancelled.

63. A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

64. A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, each of the physical blocks having a plurality of flash memory cells, each flash memory cell being individually programmable into more than two states in order to store more than one bit of data per cell, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

65. A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, each of the physical blocks having a plurality of flash memory cells, each flash memory cell being individually programmable into two states in order to store one bit of data per cell, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

DECISION ON PRELIMINARY MOTIONS
PATENT INTERFERENCE NO. 104,760

DECISION ON YAMAGAMI SECOND REQUEST FOR RECONSIDERATION AND FINAL JUDGMENT, PATENT INTERFERENCE NO. 104,760

DECISION ON APPEAL, APPEAL NO. 2001-1272

U.S. INTERNATIONAL TRADE COMMISSION, INVESTIGATION NO. 337-TA-382

DECISION ON APPEAL, *SANDISK CORPORATION V. MEMOREX PRODUCTS, INC.*, 415 F.3D 1278, 75USPQ 2D1475 (FED. CIR. 2005)

DECISION ON PRELIMINARY MOTIONS

PATENT INTERFERENCE NO. 104,760

The opinion in support of the decision being entered today
is not binding precedent of the Board.

Paper No. 91

Filed by: Motions panel
Box Interference
Washington, D.C. 20231
Tel: 703-308-9797
Fax: 703-308-7953

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

HAJIME YAMAGAMI, KOUICHI TERADA, YOSHIHIRO HAYASHI,
TAKASHI TSUNEHIRO, KUNIHIRO KATAYAMA,
KENICHI KHAKI, and TAKESHI FURUNO,

Junior Party,
(P.N. 5,644,539)

v.

ELIYAHOU HARARI, ROBERT D. NORMAN, and
SANJAY MEHROTRA,

Senior Party.
(S.N. 09/103,056)

Patent Interference No. 104,760

Before: LEE, CRAWFORD, and MEDLEY, Administrative Patent Judges.

CRAWFORD, Administrative Patent Judge.

DECISION ON PRELIMINARY MOTIONS

This interference, which was declared on October 30, 2001, with a single count, is before a motions panel for a decision on preliminary motions.

The following preliminary motions are before us:

Yamagami's preliminary motion number 1 pursuant to 37 CFR § 1.633(a) for judgment on the grounds that Harari's claims 63 and 64 are unpatentable (Paper No. 22). Opposition (Paper No. 47). Reply (Paper No. 59).

Yamagami's preliminary motion number 2 pursuant to 37 CFR § 1.633(c)(4) to designate claim 14 as not corresponding to the count (Paper No. 23). Opposition (Paper No. 48). Reply (Paper No. 60).

Yamagami's preliminary motion number 3 pursuant to 37 CFR § 1.633(f) for benefit of earlier filed applications (Paper No. 24). Opposition (Paper No. 49). Reply (Paper No. 61).

Yamagami's preliminary motion number 4 pursuant to 37 CFR § 1.633(g) attacking the benefit accorded Harari in the notice declaring this interference (Paper No. 25). Opposition (Paper No. 50). Reply (Paper No. 62).

Yamagami's preliminary motion number 5 pursuant to 37 CFR § 1.633(c)(3) to redefine the interfering subject matter by designating claims 65 and 66 as corresponding to the count (Paper No. 26). Opposition (Paper No. 51). Reply (Paper No. 63).

Yamagami's contingent preliminary motion number 6 pursuant to 37 CFR § 1.633(a) for a judgment that claims 65 and 66 are unpatentable (Paper No. 27). Opposition (Paper No. 52). Reply (Paper No. 64).

Yamagami's contingent preliminary motion number 7 pursuant to 37 CFR § 1.633(g) attacking the benefit accorded Harari in the notice declaring the interference as to newly added claims 65 and 66 (Paper No. 28). Opposition (Paper No. 53). Reply (Paper No. 65).

Yamagami's contingent preliminary motion number 8 pursuant to 37 CFR § 1.633(a) to hold claims 63 and 64 of the Harari application unpatentable (Paper No. 29). Opposition (Paper No. 54). Reply (Paper No. 66).

Harari's preliminary motion number 1 pursuant to 37 CFR § 1.633(a) for judgment that claims 9 and 14 of the Yamagami patent are not patentable (Paper No. 32). Opposition (Paper No. 41). Reply (Paper No. 55).

Harari's preliminary motion number 2 pursuant to 37 CFR § 1.633(c)(2) to redefine the interfering subject matter by adding claims 67 and 68 (Paper No. 38). Opposition (Paper No. 42). Reply (Paper No. 56).

Harari's contingent preliminary motion number 3 pursuant to 37 CFR § 1.633(c)(1) and (i) to substitute a count (Paper No. 39). Opposition (Paper No. 43). Reply (Paper No. 57).

Harari's contingent preliminary motion number 4 pursuant to 37 CFR § 1.633(f) to be accorded the benefit of the filing date of earlier applications for the added claims 67 and 68 (Paper No. 40). Opposition (Paper No. 44). Reply (Paper No. 58).

Findings of Fact

1. The count of this interference is claim 63 of the involved Harari application ("Harari application") or claim 9 of the involved Yamagami patent ("Yamagami patent"). The two claims read the same as follows:

> A storage device employing a flash memory, wherein a storage area of said storage device is divided into a plurality of physical sectors identified by physical addresses, said storage device includes:
>
> logical address conversion means which receives a logical address of data in a data writing operation and converts said logical address into a physical address, and
>
> a memory controller for receiving said physical address resulting from the conversion by the conversion means, and writing said data into a respective physical sector;
>
> wherein said logical address conversion means converts a logical address received in the writing operation to the physical address which is different from the physical address to which said logical address conversion means converted a logical address, identical to the logical address to be presently converted, in a preceding writing operation.

2. The claims of the parties which correspond to the count are:

   Yamagami: 9 and 14

   Harari: 63 and 64

3. Harari's claims 63 and 64 are identical to Yamagami's claims 9 and 14.

4. The involved Harari application (U.S. Serial No. 09/103,056) was filed on June 23, 1998.

5. The involved Yamagami patent (U.S. Patent No. 5,644,539) was filed on November 25, 1992 and issued on July 1, 1997.

6. Harari application claims 63 and 64 were copied from claims 9 and 14 of the Yamagami patent, subsequent to the filing of the Harari involved application.

7. Harari was accorded the benefit for purposes of priority of application Serial No. 07/337,566 filed April 13, 1989; application Serial No. 07/963,837 filed October 20, 1992; application Serial No. 08/249,049 filed May 25, 1994; and application Serial No. 08/931,133 filed September 16, 1997.

The subject matter of the count

8. The count in this interference is directed to a storage device which includes a flash memory which is a type of electrically erasable and programmable read-only memory or EEprom.

9. A flash memory is nonvolatile and retains its memory even after the power is shut down.

10. The storage area on the flash memory is divided into a plurality of physical sectors with physical addresses.

11. In a writing operation, a logical address conversion means converts a logical address or virtual identification information of data into a physical address on the flash memory where the data is to be written.

12. The logical address conversion means converts a particular logical address to a physical address which is different from the physical address the particular logical address was converted to in a preceding write operation.

13. A memory controller receives the physical addresses from the logical address conversion means and writes the data into a respective sector of flash memory.

The Harari involved application

14. The Harari application (Exhibit 2006) discloses a system of integrated circuit Flash EEprom chips which are under the control of a controller (page 2, lines 26-34).

15. The Flash EEprom cells on a chip are organized into sectors.

16. An object of the invention in the involved Harari application is to provide a Flash EEprom memory which remains reliable after enduring a large number of write/erase cycles (page 2, line 1 to 4).

17. One of the features of the invention of the Harari application is that it allows defect mapping at the cell level. A defective cell is replaced by a substitute cell from the same sector so that each time the defective cell is accessed, its bad data is replaced by the good data from the substitute cell (page 3, lines 26 to 29).

18. The Harari application discloses an apparatus that remaps defective cells so that the whole sector does not need to be thrown away (page 15, lines 18 to 21).

19. Each sector 401 is organized into a data portion 403 and a spare portion 405. The data portion 403 is space available to the user. The spare portion 405 is organized into an alternative defects data area 407, a defect map area 409, a header area 411 and others area 413 for use by a controller 31 to handle the defects and other overhead information (page 16, lines 23 to 32).

20. In a write operation, a comparator compares the location on the flash EEprom which is about to be written against a defect pointer map (page 29, lines 15 to 17).

21. If a defective location is pointed to, a match will exist between the address of the defective location and the defect pointer address value in the defect pointer map (page 19, lines 21 to 22).

22. When this match occurs, the memory saves the bit which is about to be written into the alternative defect data file 517 (page 22, lines 3 to 6).

23. After the bytes have been loaded into the selected memory, the controller issues a program command to the memory device and initiates a write cycle (page 22, lines 8 to 11).

24. The Harari application discloses that the collection of bits that was flagged as defective and were saved in the alternative defects data file 517 is then written in memory at the alternative defects data locations (see figure 5) thereby saving the good bit values to be used in a subsequent read. Once these data groups are written and verified, the sector write is considered completed (page 23, lines 5 to 11).

25. When the number of defective cells has exceeded the cell defect mapping's capacity for that specific sector, the whole sector is remapped (page 23, lines 12 to 15).

26. The controller marks the sector as defective and maps it to another sector with the defect pointer for the linked sectors stored in a sector defect map (page 23, lines 19-23).

27. The defect map for defective sectors may be stored in the data area of the sector, but may also be located in the controller hardware or be a part of the Flash EEprom memory (page 23, lines 29 to 31).

28. The controller compares an address given to it to access data with the defect map. If a match occurs, access to the defective sector is denied and the

corresponding substitute sector is accessed instead (page 23, lines 31 to 35).

29. The remapping can also be performed by the microprocessor. If the remapping is preformed by the microprocessor, the microprocessor looks at the incoming address and compares it against the sector defect map and if a match occurs, it substitutes the alternative location as the new command (page 24, lines 3 to 8).

The European reference

30. The disclosure of European Patent 0 392 895 A2 (Exhibit 2013)("European reference") is substantially the same as the disclosure of the involved Harari application (Yamagami Opposition to Harari Preliminary Motion No. 1, Fact No. 1; Kimura Declaration (Exhibit No. 2001, paragraph 43; Harari Reply No. 1, Fact No. 1).

Holzhammer

31. U. S. Patent No. 5,630,093 to Holzhammer (Exhibit 2014)("Holzhammer") discloses a storage device employing a flash memory array (col. 5, lines 8 to 10; col. 8, lines 5 to 10).

32. The flash memory is divided into a number of sectors (col. 4, lines 24 to 28).

33. A cluster mapping table 446, depicted in Figure 9, maps logical sectors called for by the personal computer system to the physical sectors of the flash memory array and thus forms a logical address conversion means (col. 15, lines 13 to 17).

34. A bad sector is one which contains a physical problem which prevents storage of data without errors (col. 18, lines 2 to 7).

35. The cluster map table 446 converts a logical sector called for by the personal computer system to a physical address on the flash memory which is different than the physical address previously associated with the same logical sector called for by the personal computer system in a previous writing operation. In table 446, the data in logical sector 2 called for by the personal computer system is mapped to physical sector 407. However, if physical sector 407 is a bad sector, data in logical sector 2, for example, is mapped to physical sector 443 (col. 17, line 64 to col. 18, line 63; col. 19, line 55 to col. 20, line 14).

36. A memory controller receives the physical address resulting from the conversion by the logical conversion means and writes data into a respective physical sector (col. 8, lines 14 to 41; col. 8, line 66 to col. 17, lines 16 to 20).

37. The cluster map table stores physical addresses of the physical sector into which data should be written in the next data writing operation. For example, because the physical sector 407 is a bad sector, the physical sector into which the data should be written in the next data writing operation is 443, which is stored in the cluster map table (col. 17, lines 29 to 40; col. 17, line 64 to col. 18, line 49; col. 19, line 55 to col. 20, line 14).

The declarations

The Kimura declaration

38. Yamagami has filed the declaration of Kiochi Kimura (Exhibit 2001) in support of the Yamagami preliminary motions.

39. Kimura states that the involved Harari application does not disclose or suggest the logical conversion means of the count which is included in the non-volatile memory device 29.

40. Kimura further states that as data is stored in the alternative defects file 517 an identical logical address is not converted to a different physical address than in a preceding writing operation.

41. In addition, Kimura states that the involved Harari application relates to the remapping of cells rather than sectors.

42. In regard to the European Reference, Kimura states that the European Reference does not disclose or suggest the invention recited in claims 9 and 14.

43. In regard to the Holzhammer reference, Kimura states that Holzhammer does not disclose or suggest the invention recited in claims 9 and 14 because two different logical addresses 2 and S are necessary to access two different physical addresses 407 and 421.

The Simko declaration

44. Harari has filed the declaration of Richard Simko (Exhibit 1003) in support of Harari preliminary motion 1 and the declaration of Richard Simko (Exhibit 1005) in support of Harari oppositions to Yamagami preliminary motions.

45. Simko states that the involved Harari application discloses a controller as the logical address conversion means in one embodiment and a microprocessor as the logical address conversion means in another embodiment.

46. Simko further states that the embodiment in the Harari application, wherein the microprocessor serves as the logical conversion means would have enabled one of ordinary skill in the art to make and use the invention where a microprocessor is included in the "storage device" as well.

47. In response to the statement in the Kimura declaration that data is not stored in a different physical location but in the alternative defects data file 417, Simko states that Kimura glosses over the last step in the writing process wherein the data stored in the alternative defects file is written in memory at the alternative defects data location (i.e. new physical address).

Discussion

Yamagami's Preliminary Motion number 1

This motion is entitled a "contingent" motion. However, the motion does not state the contingency. Therefore, we regard it as non-contingent.

The junior party has several sections in the motion with titles that state that there is no enabling disclosure for count 1 or Harari claims 63 and 64 as required by 35 U.S.C. § 112, first paragraph.[1]

However, within these various sections of the motion, the junior party, in addition to arguing lack of enablement, argues that the involved Harari application does not disclose a written description of the subject matter of claims 63 and 64.[2] For example, at page 11, the junior party argues :

> . . . the Harari Application (Ex 2006) does not satisfy the written description requirement of the first paragraph of 35 U.S.C. § 112 of the subject matter recited in Count 1 and copied claims 63 . . .

In addition, the junior party argues at pages 2, and 20 to 23 of the motion that claims 63 and 64 add new matter which is tantamount to an argument that the Harari application lacks written description of the subject matter recited in claims 63 and 64. Further, the Kimura declaration (Exhibit 2001) states at page 2:

---

[1] Section 112 of 35 U.S.C. applies to the claims rather than the count. Therefore, we will regard this motion as being directed to claims 63 and 64 of the involved Harari application. Harari claim 63 is identical to one of the alternatives of count 1.

[2] The description requirement found in 35 U.S.C. § 112 is separate from the enablement requirement. See Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1562, 19 USPQ2d 1111, 1115 (Fed. Cir. 1991); In re Wilder, 736 F.2d 1516, 1520, 222 USPQ 369, 372 (Fed. Cir. 1984).

> . . . the Harari application does not disclose or suggest the subject matter as per Count 1 logical address conversion means for converting of a logical address received in a present writing operation to a physical address. . .

In its preliminary motion, Yamagami also argues that Harari fails to provide a disclosure of the best mode contemplated by the Harari inventors at the time of the invention (page 8).

Accordingly, we interpret the junior party's arguments in the preliminary motion number 1 as directed to the written description requirement, the enablement requirement and the best mode requirement, despite the inaccurate headings used by Yamagami throughout its preliminary motion.[3]

Claim 63 recites:

> A storage device employing a flash memory, wherein a storage area of said storage device is divided into a plurality sectors identified by physical addresses, said storage device includes;
>
> logical address conversion means which receives a logical address of data in a data writing operation and converts said logical address into a physical address, and
>
> a memory controller for receiving said physical address resulting from the conversion by the conversion means, and writing said data into a respective physical sector;

[3] Note, that 37 CFR § 1.637(a) requires the movant to include in its motion, a statement of the precise relief requested.

wherein said logical address conversion means converts a logical address received in the writing operation to the physical address which is different from the physical address to which said logical address conversion means converted a logical address, identical to the logical address to be presently converted, in a preceding writing operation.

Written Description

A party moving for judgment on the ground that an opponent's claims corresponding to the count lack written description support in its involved application has the burden of submitting with the motion evidence which prima facie establish that the limitation or limitations in question lack either express or inherent support in the involved application. 37 CFR §§ 1.637(a); 1.639(a); Behr v. Talbott, 27 USPQ2d 1401, 1407 (Bd. Pat. App. & Int. 1992). Mere attorney argument will not suffice. Meitzner v. Mindick, 549 F.2d 775, 782, 193 USPQ 17, 22 (CCPA), cert. denied, 434 U.S. 854 (1977). The evidence may be in the form of patents, printed publications and affidavits. 37 CFR § 1.639(b).

The junior party argues that the phrases "logical address," "physical address," "logical address conversion means," "receives a logical address of data in a data writing operation and converts said logical address into a physical address" and "converts a logical address received in the writing operation to the physical address which is different from the physical address to which said logical address conversion means converted a logical address, identical to the logical address presently converted, in a

preceding writing operation" do not appear in the Harari application, and thus the specification fails to provide written description support for claim 63.

We do not find this argument to be persuasive because the test for determining compliance with the written description requirement is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter, rather than the presence or absence of literal support in the specification for the claim language. See Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1116-17 (Fed. Cir. 1991) and In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983).

As such, the junior party has the burden of establishing that the Harari application does not reasonably convey to a person of ordinary skill in the art that the inventors had possession at the time of the later claimed subject matter rather than whether the exact words of the claim can be found in the Harari application.

The junior party argues that the involved Harari application does not disclose a storage device that includes a logical address conversion means which converts a logical address to a physical address. In the junior party's view, the involved Harari application discloses that the microprocessor rather than the controller 31 converts the logical address to a physical address and that it is only the controller 31 which is disposed in the storage device.

It is true that in one of the embodiments disclosed in the Harari application, it is the microprocessor which performs the logical address conversion operation. However, the Harari application discloses at pages 23 to 24 that in one embodiment, the controller 31 is given an address to access data, and it is the controller 31 that compares this address against the sector defect map and when a match occurs, access to the defective sector is denied and the substitute address present in the defect map is entered and the substitute sector is accessed. Therefore, in this embodiment, it is indeed the controller 31 that performs the logical address conversion. We note that Yamagami's own expert admits that the controller 31 performs a logical address to physical address conversion operation in one embodiment (Exhibit 2001, page 5, paragraph 13).

The junior party also argues that the involved Harari application does not disclose any element that performs the functions performed by the logical address conversion means recited in claims 63 and 64.

We do not agree. The Harari application discloses, as detailed above, that at least the controller performs the logical address conversion.

The junior party also argues that in the device of the involved Harari application, the logical address of the preceding write operation and the logical address of the present writing operation are the same and the physical address of the present writing

operation and the preceding writing operation are the same, namely all defective cells or sectors are written into the alternative defect register 517.

We agree with the junior party that the logical address of current and preceding writing operations are the same.[4] However, while it is true that all of the data destined for defective cells is written into the alternative defect register 517 initially, the data is ultimately written into an alternative cell in the Flash EEprom. The Harari application discloses:

> In addition, the collection of bits that was flagged as defective and were saved in the alternative defects data file 516 is then written in memory at the alternative defects data locations (see figure 5), thereby saving the good bit values to be used on a subsequent read. Once these data groups are written and verified, the sector write is considered completed. (page 23, lines 5 to 11).

In our view, Harari discloses a logical address conversion means that converts a logical address to an address in an alternative defects data file and then to a physical address in the Flash EEprom memory. In this regard, we observe that claim 63 does not recite that the logical address conversion means converts a logical address directly to a physical address which is different from the physical address of the preceding writing operation.

---

[4] We note that at page 2 of the Harari application, it is disclosed that the flash memory is subjected to numerous write cycles.

The junior party further argues that the writing operation disclosed in the Harari application when the sector defect map is used is to a cell identified by the corrected address information, and not to a physical sector identified by a physical address as recited in claim 63.

This is simply not true. At page 23, Harari discloses that when the number of defective cells in the sector has exceeded the cell defect mapping capacity for that specific sector, the controller marks the sector as defective and maps it to another sector. In this way, the data destined for a defective sector is written instead into a substitute sector.[5] The sector defect map can be located in a spare area of the original defective sector or located in the controller hardware or be part of the Flash EEprom memory. In addition, as Yamagami discloses that an object of the invention is to provide a Flash EEprom memory system that remains reliable after enduring a large number of write cycles, it is implicit in the disclosure of the involved Harari application that there are successive write operations.

In view of the foregoing, it is our determination that the junior party has failed to meets its burden of establishing that the involved Harari application disclosure does not

[5] We note that when sector remapping is done, the defective sector is not accessed but rather the substitute sector (which is different than the sector accessed in a preceding write operation) is accessed instead.

provide a written description of the subject matter of claim 63 as required by 35 U.S.C. § 112.

Yamagami argues that there is no disclosure of the subject matter of claim 64 because the Harari application does not disclose or suggest the features recited in claim 63, and as such, does not disclose or suggest the features of claim 64 which is dependent on claim 63. In addition, Yamagami argues that claim 64 recites that the write sector pointer is a further element of the storage device, not an element which forms a part of the logical address to physical address conversion means.

Claims 64 recites:

> A storage device employing a flash memory according to claim 63, further comprising:
> a write sector pointer for storing said physical address of the physical sector into which data should be written in the next data writing operation,
> wherein said logical address conversion means converts said logical address into said physical address stored in said write sector pointer.

As we detailed above in our discussion of the written description of the subject matter of claim 63, it is our opinion that the junior party has failed to prove that the involved Harari application does not describe the features of claim 63. In addition, we agree with the senior party that the involved Harari application does disclose a write sector pointer in the form of defect pointers at page 23, lines 19 to 20. These defect pointers, which correspond to addresses for substitute sectors (the sector into which

data should be written in the next data writing operation) are stored in the sector defect map. This sector defect map may be stored in another memory maintained by the controller or in the original defective sector and thus not form a part of the controller which forms the logical address physical address conversion means (page 23, lines 27 to 31).

Enablement

The junior party argues that the Harari application fails to enable a person of ordinary skill in the art to make and use the subject matter of claim 63. To prevail on a motion for judgment that a party's application lacks an enabling disclosure, the moving party must show that the disclosure would not enable a person of ordinary skill in the art to make or use the invention without undue experimentation on their part. See In re Donohue, 550 F.2d 1269, 1271, 193 USPQ 136, 137 (CCPA 1977). The burden of proof is on the moving party who must show lack of enablement by a preponderance of the evidence. Kubota v. Shibuya, 999 F.2d 517, 519 n.2, 27 USPQ2d 1418, 1421 n.2 (Fed. Cir. 1993); Field v. Knowles, 183 F.2d 593, 596, 86 USPQ 373, 375 (CCPA 1950).

In regard to the lack of enablement argument, Yamagami addresses what is actually disclosed in the Harari application, but fails to include a discussion of whether a person could make or use the invention without undue experimentation.

The mere absence of disclosure does not per se establish lack of enablement. An inventor need not explain every detail since the inventor is speaking to those skilled in the art. In re Howarth, 654 F.2d 103, 105, 210 USPQ 689, 691 (CCPA 1981). Rather, the question is whether a person of ordinary skill in the art coupled with knowledge known in the art would have been enabled to make and use the invention without undue experimentation.

As the junior party has not addressed whether a person skilled in the art could make or use the invention without undue experimentation, this portion of the motion fails because the junior party has failed to meet its burden.

Best Mode

Yamagami also argues that the Harari application fails to disclose a best mode. The best mode provision of § 112 speaks in terms of the best mode "contemplated by the inventor," there is no objective standard by which to judge the adequacy of the best mode disclosure. Instead, only evidence of "concealment," whether accidental or intentional, is considered. DeGeorge v. Bernier, 768 F.2d 1318, 1324, 226 USPQ 758, 763 (Fed. Cir. 1985). The specificity of the disclosure required to comply with the best mode requirement must be determined by the knowledge of the facts within the possession of the inventor at the time of the filing of the application. See United States Dep't of Energy v. Daugherty, 687 F.2d 438, 446, 215 USPQ 4, 11 (CCPA 1982).

Yamagami has not discussed what mode of practicing the invention was regarded by Harari as best. In addition, Yamagami has failed to address the issue of concealment. As such, this portion of this motion fails.

In view of the foregoing, the junior party's preliminary motion for a judgment pursuant to CFR § 1.633(a) that claims 63 and 64 of the Harari application are unpatentable is denied.

Yamagami's Preliminary Motion number 2

This motion is entitled a "contingent" motion. However, the motion does not state the contingency. Therefore, we regard this motion as non-contingent.

Yamagami's preliminary motion number 2 seeks to designate claim 14 as not corresponding to the count.

Claim 14 recites:

> A storage device employing a flash memory according to claim 9, further comprising:
> a write sector pointer for storing said physical address of the physical sector into which data should be written in the next data writing operation,
> wherein said logical address conversion means converts said logical address into said physical address stored in said write sector pointer.

Yamagami has the burden of proving that claim 14 of the Yamagami patent does not define the same patentable invention as any Harari claims ("designated claims") designated in the notice declaring the interference as corresponding to the count that

Yamagami does not dispute. 37 CFR § 1.637(c)(4)(ii). Section 1.601(n) of 37 CFR reads in pertinent part as follows:

> . . .Invention "A" is a *separate patentable invention* with respect to invention "B" when invention "A" is new (35 U.S.C. 102) and non-obvious (35 U.S.C. 103) in view of invention "B" assuming invention "B" is prior art with respect to invention "A".

Therefore, Harari's designated claims are treated as prior art for purposes of this analysis.

Mere reference to a claimed feature which is not disclosed by the prior art and not included in the Count does not per se establish "separate patentability" within the meaning of § 1.601(n). Rather, the question is whether the inclusion of the feature would have rendered the claim nonobvious to a person of ordinary skill in the art. See L'Esperance v. Nishimoto, 18 USPQ2d 1534, 1538 (Bd. Pat. App. Int. 1989). Therefore, Yamagami has the burden of establishing, by a preponderance of the evidence, that its claim 14 is patentably distinct with respect to each of Harari's involved claims in accordance with the guidance set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966); 37 CFR § 1.637(c)(4)(ii); § 1.601(n).

Yamagami's motion is misdirected to whether the examiner in the interference memo established that the subject matter recited in claim 14 would have been obvious. Claim 14 was designated as corresponding to the count in the interference declaration issued by the Administrative Patent Judge ("APJ") that declared this interference. As

such, the designation of claim 14 as corresponding to the count was an interlocutory order issued by the APJ which is presumed correct. The burden of showing that an interlocutory order should be modified is on the party attacking the order. 37 CFR § 1.655(a). Yamagami, as the movant, bears the burden to prove that the subject matter recited in claim 14 is not the same or obvious over each of Harari's involved claims. This Yamagami has not done.

In response to the examiner's determination that U.S. Patent No. 4,829,425 to Bain ("Bain") discloses write pointers, Yamagami argues that a write sector pointer for storing a physical address of the physical sector into which data should be written in the next writing operation as set forth in claim 14, is not suggested or taught by the count (which is identical to Harari's claim 63) or the Bain reference. Yamagami further argues that Bain does not address a next data writing operation and has no discussion of a write sector pointer in combination with logical address conversion means that converts the logical address into the physical address stored in the write sector pointer as set forth in claim 14.

However, even if a feature is not taught in the prior art, Yamagami still must establish that the inclusion of the feature would not have been obvious to a person of ordinary skill in the art. While Yamagami argues in a conclusory matter that there is no evidence of a motivation to combine the Bain register set pointers with the subject matter of Harari's claim 63, Yamagami has not met its burden that there is no

motivation to make the combination. In fact, Yamagami has not discussed the set pointers of Bain in any detail.

Yamagami concludes that as there is no showing by the examiner that Yamagami claim 14 is the same invention as Harari claim 63, Yamagami claim 14 should be designated as not corresponding to the count. As discussed above, the analysis fails to sufficiently meet Yamagami's burden to establish that claim 14 is not the same invention as Harari claim 63. It is Yamagami who must demonstrate nonobviousness. A lack of showing by the examiner of the opposite does not make the case for Yamagami.

In response to the senior party's argument in the opposition to this motion that Holzhammer discloses write sector pointers, Yamagami merely argues that Holzhammer does not disclose or suggest the conversion of a logical address which is different from the physical address to which the same logical address is converted in a preceding writing operation. However, this subject matter is recited in Harari claim 63. Yamagami concludes in the reply that Holzhammer does not disclose or suggest the subject matter of claim 14. The only portion of the reply which is directed to the combination of Holzhammer and the subject matter of Harari claim 63 is a conclusory statement that there is no showing of how the respective features of Holzhammer can be combined with the count (which is the same as Harari claim 63). Yamagami does

not discuss in any meaningful way why the teachings of Holzhammer cannot be combined with the subject matter of the Harari claim 63.

In response to the senior party's argument in the opposition to this motion that the European reference discloses write sector pointers, Yamagami argues in the reply that the European reference does not disclose or suggest a write sector pointer for storing the physical address of the physical sector into which data should be written in the next writing operation. Yamagami has not addressed what the combination of the European reference and Harari claim 63 would suggest to a person of ordinary skill. Yamagami merely states that there is no showing of how the European reference may be combined with the subject matter of Harari claim 63 or the motivation to make such a combination. The problem, however, is that it is Yamagami who has to make a showing of the opposite.

Furthermore, Yamagami makes no representation that it is not aware of any additional prior art which would render obvious Yamagami claim 14 when taken in view of a Harari claim designated as corresponding to the count in light of the additional prior art. The absence of such representation, is an additional ground of why Yamagami has not sustained its burden of proving that its claim 14 should not correspond to the count.

This motion is denied because Yamagami has failed to meet its burden of establishing that the subject matter of claim 14 would not have been obvious in view of

the subject matter of those involved Harari claims whose correspondence to the count Yamagami does not dispute.

Yamagami's Preliminary Motion number 3

Yamagami's preliminary motion number 3 seeks an order according benefit for purposes of priority of earlier filed applications: Japanese Patent Application No. 3-310848, filed November 26, 1991; Japanese Patent Application No. 3-314297, filed November 28, 1991 ; Japanese Patent Application No. 4–031756, filed February 19, 1992 and Japanese Patent Application No. 4-099891, filed April 20, 1992 under 37 CFR § 1.633(f). This motion is unopposed. The motion is granted.

Yamagami's Preliminary Motion number 4

In this preliminary motion, Yamagami attacks the benefit accorded Harari in the notice declaring this interference of : U.S. Patent Application Serial No. 07/337,566; U.S. Patent Application Serial No. 07/963,837; U.S. Patent Application Serial No. 08/249,049; and U. S. Patent Application Serial No. 08/931,133. Yamagami argues that the subject matter of claims 63 and 64 is not disclosed in the Harari benefit applications in such a matter as to enable a person of ordinary skill to make or use the invention. In this motion, like in preliminary motion number 1, Yamagami has failed to address the issues of whether a person of ordinary skill in the art could make or use the invention without undue experimentation and as such has failed to establish that a

person of ordinary skill in the art would not have been enabled by the above-listed benefit applications. As such, this motion is denied.

Yamagami's Preliminary Motion number 5

This motion is entitled a "contingent" motion. However, the motion does not state the contingency. Therefore, we will regard it as noncontingent.

Yamagami's preliminary motion number 5 seeks to redefine the interfering subject matter by an order stating that claims 65 and 66 of the involved Harari application correspond to the count. This motion is unopposed. This motion is granted.

Yamagami's Contingent Preliminary Motion number 6

Yamagami's preliminary motion number 6 seeks a judgment that Harari claims 65 and 66 are unpatentable and is contingent upon the granting of Yamagami's preliminary motion number 5. Yamagami's argument is that since the involved Harari application lacks an enabling disclosure of the subject matter of claim 63 from which claims 65 and 66 depend, the Harari application lacks an enabling disclosure of the subject matter of claims 65 and 66 as well. In view of the junior party's failure to prove that the involved Harari application does not provide a disclosure that satisfies both the written description and enablement requirement of 35 U.S.C. § 112, first paragraph, with regard to claim 63 as set out in detail in our discussion of Yamagami's preliminary motion number 1, this motion is denied.

Yamagami's Contingent Preliminary Motion number 7

Yamagami's preliminary motion number 7 attacks the benefit afforded Harari in the notice declaring the interference and is contingent upon the granting of Yamagami's preliminary motion number 5. Yamagami argues that claims 65 and 66 are not entitled to the benefit of the filing dates of: Application Serial No. 07/337,566, filed April 13, 1989; Application Serial No. 07/337,566, filed April 13, 1989; Application Serial No. 07/963,837, filed October 20, 1992; Application Serial No. 08/249,049, filed May 25, 1994; and Application Serial No. 08/931,133, filed September 16, 1997. Yamagami reasons that since the involved Harari application does not include an enabling disclosure of claims 65 and 66, the Harari benefit applications likewise do not include an enabling disclosure since the Harari benefit applications are similar in content to the involved Harari application.

However, the issue is not whether the benefit applications include an enabling disclosure of the subject matter of claims 65 and 66, rather the issue is whether the benefit applications describe an embodiment within the scope of the count. Hunt v. Treppschuh, 523 F.2d 1386, 1389, 187 USPQ 426, 429 (CCPA 1975); see also Weil v. Fritz, 572 F.2d 856, 865 n.16, 196 USPQ 600, 608 n.16 (CCPA 1978). An earlier filed application need not describe all species the count encompasses. Utter v. Hiraga, 845 F.2d 993, 998, 6 USPQ2d 1709, 1714 (Fed. Cir. 1988). Therefore, in order for Yamagami to establish that claims 65 and 66 are not entitled to the filing date of

Application Serial No. 07/337,566, filed April 13, 1989, Yamagami must prove that Application Serial No. 07/337,566 does not describe an embodiment within the scope of the count. Such proof is also necessary to establish that Harari is not entitled to the filing dates of: Application Serial No. 07/963,837, filed October 20, 1992; Application Serial No. 08/249,049, filed May 25, 1994; and Application Serial No. 08/931,133, filed September 16, 1997. We note that Yamagami has not addressed the disclosures of the above-listed benefit applications with regard to Harari claims 63 and 64 which recite embodiments within the scope of the count.

Yamagami has not shown that the earlier filed Harari applications do not describe an embodiment within the scope of the count. As such, this motion is denied.

Yamagami's Contingent Preliminary Motion number 8

In this preliminary motion, Yamagami seeks a judgment that claims 63 and 64 of the involved Harari application are unpatentable based upon the granting of Yamagami's preliminary motion number 4. In preliminary motion number 4, Yamagami attacks the benefit accorded Harari in the notice declaring the interference of U.S. Applications Serial Nos. 07/337,566; 07/963,837; 08/249,049 and 08/931,133. In preliminary motion number 8, Yamagami reasons that if Harari claims 63 and 64 are not accorded the benefit of the filing dates of the above noted applications, the Yamagami patent is prior art to Harari claims 63 and 64. We note that Yamagami has confused benefit for the purposes of establishing priority of invention (35 U.S.C. § 119) with

benefit for purposes of establishing patentability over prior art (35 U.S.C. § 120). In any case, as preliminary motion number 4 was denied and therefore, the contingency did not materialize, Yamagami's contingent preliminary motion number 8 is dismissed.

Harari's Preliminary Motion number 1

In Harari's preliminary motion number 1, Harari seeks judgment under 37 CFR § 1.633(a) because in Harari's view, the Yamagami claims 9 and 14 are unpatentable under 35 U.S.C. § 102(b) as anticipated by the European Patent Application Publication No. 0 392 895 A2 (Harari Exhibit 1001)("European patent") and Holzhammer.[6]

Harari argues that claims 9 and 14 of the Yamagami patent are anticipated by the European patent. Yamagami has admitted that the disclosure of the European patent is substantially the same as the Harari application (Yamagami's Opposition to Harari preliminary motion number 1, Fact No. 1).

In response to this motion, Yamagami argues that the European patent does not anticipate Yamagami claims 9 and 14. Yamagami argues that the European patent does not disclose that the logical address conversion means is disposed in the storage device and that the European patent relates to cell remapping rather than sector remapping. Yamagami also argues that the European patent does not explicitly or

---

[6] Holzhammer and the European patent are not prior art to Harari.

implicitly disclose a storage device employing a flash memory, wherein a storage area of the storage device is divided into a plurality of physical sectors identified by physical addresses. Further, Yamagami argues that the European patent does not disclose explicitly or implicitly conversion of a logical address of a present writing operation to a physical address different from the physical address converted from the logical address in a preceding writing operation. These are the same arguments Yamagami made in its preliminary motion number 1 in regard to the involved Harari application. We refer the parties to that discussion for details of our opinion in this regard.

We are of the opinion that the European patent discloses sector remapping (Exhibit 1001, col. 2, lines 10 to 13; col. 5, lines 9 to 14; col. 6, lines 11 to 13 and 17 to 20; col. 15, lines 17 to 20). In addition, the European patent discloses a logical address conversion means disposed in a storage device (Exhibit 1001, col. 15, lines 24 to 50). Although the data is temporarily stored in the alternative defects data file 517, it is ultimately stored in memory at the alternative data defects location which is a different physical address converted from the logical address in the preceding writing operation. Therefore, the European patent does disclose conversion of a logical address of a present writing operation to a physical address different from the physical address converted from the logical address in a preceding writing operation.

In regard to Holzhammer, we agree with the senior party that Holzhammer discloses the subject matter of Yamagami's claims 9 and 14.

Yamagami argues that Holzhammer discloses that a first logical address is converted to a first physical address and that a second subsequent different logical address is converted to a second different physical address in a subsequent conversion step. We do not agree.

Holzhammer discloses at column 18, lines 32 to 58 that logical address 2 is converted to physical address 407 in a first conversion operation and to physical address 443 in a subsequent conversion operation.

Yamagami also argues that there is no disclosure in Holzhammer of memory controller as is recited in Yamagami claim 9.

We do not agree. Holzhammer discloses a controller 92 which controls the structure of the flash memory array (col. 8, line 66 to col. 9, line 5).

In regard to claim 14, Harari argues that since the cluster mapping table 446 seen in Figure 9 is a table comprised of a plurality of linked-list entries associating logical addresses with physical addresses, Holzhammer discloses a write sector pointer which stores the physical address of the physical sector into which data should be written in the next data writing operation, as recited in claim 14.

Yamagami argues that the cluster mapping table 446 in Holzhammer maps a logical address to a logical address and that the physical address is not stored in the cluster mapping table 446.

As seen in Figure 9, this is not true. A logical address 2 is converted to physical addresses 407 and 443 e.g. and the physical addresses are indeed stored on the cluster mapping table 446. As such, we agree with the senior party that Holzhammer does indeed disclose a write sector pointer.

The motion is granted.

Harari's Responsive Preliminary Motion number 2 and Contingent Preliminary Motions 3 and 4

In Harari's responsive preliminary motion number 2, Harari seeks to add claims 67 and 68 in an attempt to eliminate the arguments posed in Yamagami's preliminary motion numbers 1, 4 and 6. In view of our denial of Yamagami's preliminary motion numbers 1, 4 and 6, we dismiss Harari's preliminary motion number 2.

Harari's preliminary motions numbers 3 and 4, which are contingent upon the granting of Harari preliminary motion number 2 and Yamagami's motion numbers 1, 4 and 6, which were all denied, are dismissed.

Order to Show Cause

The preliminary statements are open on the record. According to the preliminary statements, Harari's filing date, which is a constructive reduction to practice, is April 13, 1989, while Yamagami's conception as well as reduction to practice date is November

26, 1991. Therefore, Yamagami is given **twenty days (20)** from the date of this paper to show cause why judgment should not be entered against Yamagami.

Jameson Lee
Administrative Patent Judge

Murriel E. Crawford
Administrative Patent Judge

Sally C. Medley
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

MEC/tdl

cc: (via Federal Express)

Counsel for YAMAGAMI:

Carl I. Brundidge, Esq.
ANTONELLI, TERRY, STOUT and KRAUS, LLP
1300 North Seventeenth Street
Suite 1800
Arlington, VA 22209

Tel: 703-312-6600
Fax: 703-312-6666

Counsel for HARARI:

Gerald Parsons, Esq.
PARSONS HSUE & de RUNTZ LLP
655 Montgomery Street
Suite 1800
San Francisco, CA 94111

Tel: 415-318-1160
Fax: 415-693-0194

DECISION ON YAMAGAMI SECOND REQUEST FOR RECONSIDERATION AND FINAL JUDGMENT, PATENT INTERFERENCE NO. 104,760

The opinion in support of the decision being entered
today is not binding precedent of the Board

Filed by: Trial Section Merits Panel
Mail Stop Interference
Board of Patent Appeals and Interferences
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
Tel: 703-308-9797
Fax: 703-305-0942

Paper No. 97

Filed
29 May 2003

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

HAJIME **YAMAGAMI**, KOUICHI TERADA, YOSHIHIRO HAYASHI,
TAKASHI TSUNEHIRO, KUNIHIRO KATAYAMA,
KENICHI KHAKI, and TAKESHI FURUNO,
Junior Party,
(Patent 5,644,539),

v.

ELIYAHOU **HARARI**, ROBERT D. NORMAN and
SANJAY MEHROTRA,
Senior Party,
(Application 09/103,056).

Patent Interference No. 104,760

Before LEE, CRAWFORD and MEDLEY, Administrative Patent Judges.

MEDLEY, Administrative Patent Judge.

DECISION ON YAMAGAMI SECOND REQUEST FOR RECONSIDERATION AND FINAL JUDGMENT

A. Introduction

A decision on preliminary motions was entered 18 April 2003. In our decision, Yamagami was ordered to show cause why judgment should not be entered against it (Paper 91 at 35). In response to the show cause order, Yamagami filed a request for reconsideration of our decision on preliminary motions (Paper 93). Yamagami s request for reconsideration was dismissed for procedural errors, without prejudice to file another request for reconsideration (Paper 94).

On 20 May 2003, Yamagami filed a second request for reconsideration (Paper 95). Yamagami seeks reconsideration of that part of our decision on preliminary motions in which we (1) denied Yamagami Preliminary Motion 1 for judgment against Harari based on 35 U.S.C. § 112, ¶ 1, and (2) granted Harari Preliminary Motion 1 for judgment against Yamagami on the grounds that Yamagami s involved claims are unpatentable based on prior art.

B. Discussion

A party requesting reconsideration of an interlocutory decision must specify with particularity points believed to have been misapprehended or overlooked in rendering the decision. 37 CFR § 1.640(c). A request for reconsideration is not a new opportunity to raise issues which should have been raised during the preliminary motions period. Further, a request for reconsideration will not be granted where the moving party merely disagrees with the decision of the panel.

Yamagami argues that we overlooked or misapprehended Yamagami s arguments and evidence of record that Harari did not provide written description support for Harari claims 63

and 64 (Recon.[1] 2). In essence, Yamagami asserts that we did not consider that portion of Yamagami preliminary motion 1 where Yamagami argued that Harari lacked written description support for Harari claims 63 and 64. However, as is evident from our seven page discussion addressing Yamagami s written description arguments, the panel did consider Yamagami s arguments and the evidence that Yamagami directed us to in support of its arguments. Yamagami, as the requestor for reconsideration of our decision on preliminary motions, must demonstrate how we specifically misapprehended or overlooked an argument made, or evidence relied upon in support of an argument. A general argument such as that made by Yamagami does not provide a basis upon which relief will be granted.

Yamagami argues that there is insufficient detailed description of how to make or use the controller 31 to perform the claimed conversion with respect to sector remapping (Recon. 3-4). Yamagami argues that it set forth this point in its preliminary motion through certain Material Facts, in its argument section of the motion, in certain paragraphs of the Kimura declaration, and in its reply 1[2] (Recon. 3-4). We find no such argument made by Yamagami in the argument section of its preliminary motion 1. To the extent that Yamagami now directs us to statements of facts in Yamagami preliminary motion 1 and passages in the Kimura declaration in support of the new argument, it is too late. We note that in the argument section of Yamagami preliminary motion 1, there is not a single citation to the Kimura declaration, or to any statement of fact. It is

---

[1] Recon. refers to Yamagami s second request for reconsideration, i.e. Paper 95.

[2] In its request for reconsideration, Yamagami argues that it raised the issue on page 5, line 29 thru page 7. (Recon. 4). We assume that Yamagami is referring to its reply 1, since the reply 1 matches the description given by Yamagami.

not the role of the board to play detective with a party s evidence or statements of facts and come up with an argument for the party. That is the role of counsel, not judge. Yamagami should have directed our attention to any statements of facts or to paragraphs of the Kimura declaration in its argument section of its motion. It is too late for Yamagami to do so now. Note further, that incorporation by reference of arguments is not permitted. See Paper 1, Standing Order § 13. Furthermore, in deciding Yamagami preliminary motion 1, we did not consider Yamagami s reply. Because Yamagami s preliminary motion 1 failed to set forth a prima facie case for entitlement to relief, Harari s opposition to Yamagami s preliminary motion 1 was not considered. Consequently, Yamagami s reply need not have been considered. In any event, we have considered the statements of facts, paragraphs in the Kimura declaration and arguments made in Yamagami reply that Yamagami now direct us to and do not find the argument now advanced, i.e. that there is insufficient detailed description of how to make or use the controller 31 to perform the claimed conversion with respect to sector remapping.

Yamagami argues that our statement on page 17, lines 2-11 of our decision that we note that Yamagami s own Expert admits that the controller 31 performs a logical address to a physical address conversion operation in one embodiment (Exhibit 2001, page 5, paragraph 13) is not true. Yamagami argues that there is no admission by Kimura at any point in his declaration (Recon. 4). We agree that paragraph 13 of the Kimura declaration does not support the statement made in our decision. Accordingly, we modify the decision, by deleting lines 8-11 on page 17, beginning with We note.... The change to our decision to delete the above noted sentence, however, does not change the overall outcome of our decision to deny Yamagami preliminary motion 1.

Yamagami argues that the panel erred when it attributed the stated feature in the Harari specification of providing a flash EEPROM memory which remains reliable after enduring a large number of write/erase cycles to cell and sector defect re-mapping. Yamagami argues that Harari s sector remapping is conditional, in that it only occurs after a defective sector is detected and would not satisfy the written description requirement for prolonging life (Recon. 4-5).

There are several problems with Yamagami s argument. First, we did not attribute reliability to the sector remapping embodiment. We said in our decision that as Yamagami discloses that an object of the invention is to provide a Flash EEprom memory system that remains reliable after enduring a large number of write cycles, it is implicit in the disclosure of the involved Harari application that there are successive write operations. Yamagami does not argue that Harari does not perform successive write operations, or that the sector remapping is not performed in two consecutive write operations. Rather, Yamagami argues that the remapping (conversion) is not done every time there is a write operation.

Yamagami made this argument in its reply 1 (Reply 1 at 6, lines 4-6) and in its opposition to Harari s preliminary motion 1. However, in deciding Yamagami preliminary motion 1, we did not consider Yamagami s reply or Yamagami s opposition to an unrelated motion. Because Yamagami s preliminary motion 1 failed to set forth a prima facie case for entitlement to relief, Harari s opposition to Yamagami s preliminary motion 1 was not considered. Consequently, Yamagami s reply need not have been considered. That Yamagami made the argument in an opposition to an unrelated motion is without merit. We will not, at this late stage in the proceedings, consider arguments Yamagami made in an unrelated opposition to an unrelated motion. Moreover, as stated above, incorporation of arguments is not permitted.

In any event, we note that Harari claims 63 and 64 are not limited to performing a conversion for every write operation. The claims are broad enough to include performing a conversion at some point in time between two consecutive write operations. Furthermore, lacking from the claim language of Harari claims 63 and 64 is a requirement that the conversion act to prolong the life of the memory.

Yamagami argues that we misapprehended or overlooked statements made by Kimura and arguments advanced by Yamagami in its preliminary motion 1 that it is inherently obvious that undue experimentation (although this term is not specifically used) would be required to practice the apparatus as disclosed in the Harari specification ... (Recon. 5). As stated above, Yamagami does not, in the argument section of Yamagami preliminary motion 1, direct our attention to any passage in the Kimura declaration. Yamagami cannot now direct us to passages in the Kimura declaration with the hopes that we will consider those passages. It is too late. Consideration of such evidence would be prejudicial to Harari. In any event, it is not enough to allege, or for a declarant to state that experimentation would be required to practice an invention, or even that undue experimentation would be required without sufficient supporting evidence to back up the argument or statement.

Yamagami argues that we erred in not giving deference to the examiner s determination that Yamagami s claims were patentable over the subject matter of the European patent application and Holzhammer (Recon. at 5). We are not bound by decisions made by an examiner during ex parte prosecution. During an interference, independent review of issues are made. See Glaxo Wellcome, Inc. v. Cabilly, 56 USPQ2d 1983, 1984 (BPAI (ITS)). (Neither the Board nor a party are bound by an ex parte decision made during prosecution by another party.

A motion in an interference is not an appeal from the examiner's decision, but an independent request to the Board). Accordingly, we did not overlook the examiner s determination made during ex parte prosecution of the Yamagami involved patent. Instead, we reviewed Harari preliminary motion 1, Yamagami opposition 1, and the evidence related to the motion and opposition in making our decision.

Yamagami argues that we failed to mention, in our decision, that Harari has a burden to overcome in order for it to prove anticipation (Recon. 6). It is not necessary for an opinion to state the obvious. Rule 637(a) provides that the movant bears the burden to demonstrate that it is entitled to the relief requested. That we did not quote the rule in our decision does not mean that Harari was exempt from meeting its burden of proof. Yamagami has failed to sufficiently demonstrate that we ignored the burden in rendering our decision. By addressing Yamagami s opposition 1, it is inherent that the panel determined that Harari met its burden to demonstrate that it was entitled to the relief requested in the first place. Accordingly, we see no reason to amend our decision.

Yamagami disagrees with our determination that the European patent discloses sector re-mapping. Mere disagreement with a determination made by the panel is insufficient reason to grant a request for reconsideration.

Having considered Yamagami s arguments in its request for reconsideration, we grant Yamagami s request for reconsideration with respect to that portion of our decision on page 17, lines 8-11, by deleting the following: [w]e note that Yamagami s own expert admits that the controller 31 performs a logical address to physical address conversion operation in one

embodiment (Exhibit 2001, page 5, paragraph 13). As noted above, the deletion does not change our decision to deny Yamagami preliminary motion 1.

Having considered Yamagami s additional arguments, we conclude that Yamagami has failed to demonstrate that we misapprehended or overlooked any fact or argument first presented prior to the filing of the request for reconsideration. Accordingly, Yamagami s request for reconsideration is **granted-in-part**.

Since Yamagami is a junior party who has failed to overcome the effective filing date of the senior party Harari, judgment is entered against Yamagami.

Upon consideration of the record, it is

ORDERED that Yamagami s request for reconsideration is **granted-in-part**;

FURTHER ORDERED that judgment as to Count 1 (Paper 1 at 5), the sole count in the interference, is awarded against junior party HAJIME YAMAGAMI, KOUICHI TERADA, YOSHIHIRO HAYASHI, TAKASHI TSUNEHIRO, KUNIHIRO KATAYAMA, KENICHI KHAKI, and TAKESHI FURUNO;

FURTHER ORDERED that junior party HAJIME YAMAGAMI, KOUICHI TERADA, YOSHIHIRO HAYASHI, TAKASHI TSUNEHIRO, KUNIHIRO KATAYAMA, KENICHI KHAKI, and TAKESHI FURUNO is not entitled to a patent containing claims 9 and 14 (corresponding to Count 1) of patent 5,644,539;

FURTHER ORDERED that a copy of this paper shall be made of record in files application 09/103,056 and U.S. Patent 5,644,539;

FURTHER ORDERED that if there is a settlement agreement, attention is directed to 35 U.S.C. § 135 (c) and 37 CFR § 1.661.

JAMESON LEE
Administrative Patent Judge

MURRIEL E. CRAWFORD
Administrative Patent Judge

SALLY C. MEDLEY
Administrative Patent Judge

cc (via e-mail):

Attorney for Yamagami:

Carl I. Brundidge (cbrundidge@antonelli.com)
Frederick D. Bailey (fbailey@antonelli.com)
David O. Oren (doren@antonelli.com)

Attorney for Harari:

Gerald P. Parsons (gparsons@phdr-law.com)

DECISION ON APPEAL, APPEAL NO. 2001-1272

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ELIYAHOU HARARI, ROBERT D. NORMAN, and SANJAY MEHROTRA

Appeal No. 2001-1272
Application No. 09/056,398

ON BRIEF[1]

Before RUGGIERO, BLANKENSHIP, and SAADAT, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 63-67, which are all the claims remaining in the application.

We reverse.

[1] Appellants waived oral hearing (Paper No. 28).

BACKGROUND

The invention relates to programming and erasing of electronically erasable programmable read only (EEprom) cells. Claim 63 is reproduced below.

63. A method of treating at least one erased EEprom cell, comprising:

a) accessing a number of control gates and accessing a bit line, thereby activating a number of memory cells, each of said memory cells having a source, a drain, and a control gate;

b) subsequent to accessing said bit line, sensing the presence of at least one activated cell from said number of memory cells that is erased to a state other than one of at least two data states; and

c) subsequent to sensing the presence of said erased cell, applying a first voltage to said bit line, a second voltage to said control gate of at least said erased cell, and a third voltage to said source of at least said erased cell, said first and second voltages being higher than said third voltage.

Claims 63-67 stand rejected under 35 U.S.C. § 112, first paragraph.

We refer to the Final Rejection (Paper No. 16) and the Examiner's Answer (Paper No. 22) for a statement of the examiner's position and to the Brief (Paper No. 21) and the Reply Brief (Paper No. 23) for appellants' position with respect to the claims which stand rejected.

OPINION

At the outset, we note our agreement with appellants (e.g., Brief at 4) that the issue in the instant appeal is whether or not the instant claims pass muster under 35 U.S.C. § 112, first paragraph. In the instant proceeding, it is irrelevant whether or not a

claim before us defines the same patentable invention as a claim in the U.S. patent with which appellants have requested an interference. We thus make our determinations independent of any inquiry into whether the instant application and the patent claim interfering subject matter.

The initial statement of the rejection (Answer at 2) could be interpreted as being based on an alleged lack of enablement for the claimed subject matter. However, in view of the discussion between the examiner and appellants, we conclude that the rejection is based on an alleged lack of written description support for the subject matter now claimed.

We further note that the initial statement of the rejection alleges lack of support for language that does not appear in the claims before us. Since our review of the rejection is confined to the requirements of 35 U.S.C. § 112, first paragraph, we find the allegations that the disclosure does not provide support for language that is not in the claims to be misplaced. The disclosure need not provide support for language that is not in the claims.

In any event, the "Response to Argument" section of the Answer (at 2-5) asserts that steps (b) and (c) of claim 63 are not supported by the instant disclosure. Appellants' position (Brief at 4-6) is that the steps are described in a preliminary amendment to the written description and in instant Figure 23, added by the preliminary

amendment.[2] In particular, appellants refer (Brief at 5) to material describing "another feature of the invention," in which, subsequent to the erasing of a memory cell, the cell is "programmed slightly" to bring the cell to the state with the lowest threshold level (ground state) adjacent to the "erased" state. Appellants assert that claimed steps (b) and (c) correspond to steps 4 through 6 of Figure 23.

The examiner responds (Answer at 3-4) that the verification of step 5 is to check whether or not the addressed cells reach the program state, not the "erased" state. In the examiner's view, it follows that the voltages recited in step (c) are not applied, because the claim requires that the voltages be applied "subsequent to sensing the presence of said erased cell."

To comply with the "written description" requirement of 35 U.S.C. § 112, first paragraph, an applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention. The invention is, for purposes of the "written description" inquiry, whatever is now claimed. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991).

The invention claimed does not have to be described in ipsis verbis in order to satisfy the description requirement of 35 U.S.C. § 112, first paragraph. Union Oil Co. v.

[2] Although couched in terms of the "effective filing date of the present application," apparently the examiner has determined that the material added by preliminary amendment to the written description and drawings is to be accorded benefit of a filing date earlier than the presentation of claims 63 through 67 because of an incorporation by reference appearing in a parent application. (See Paper Nos. 10 and 11.) Accordingly, we will consider the preliminary amendment as if part of the disclosure.

Atlantic Richfield Co., 208 F.3d 989, 1000, 54 USPQ2d 1227, 1235 (Fed. Cir. 2000), cert. denied, 531 U.S. 1183 (2001). However, one skilled in the art, reading the original disclosure, must be able to immediately discern the limitations now claimed. See Waldemar Link GmbH & Co. v. Osteonics Corp., 32 F.3d 556, 558, 31 USPQ2d 1855, 1857 (Fed. Cir. 1994) ("The fact finder must determine if one skilled in the art, reading the original specification, would immediately discern the limitation at issue in the parent.") Further, however, the question of written description support should not be confused with the question of what would have been obvious to the artisan. Whether one skilled in the art would find the instantly claimed invention obvious in view of the disclosure is not an issue in the "written description" inquiry. In re Barker, 559 F.2d 588, 593, 194 USPQ 470, 474 (CCPA 1977).

With these guidelines in mind, we find that appellants have pointed to material in the disclosure that is sufficient to meet the "written description" requirement of 35 U.S.C. § 112, first paragraph for the subject matter of instant claim 63. In particular, we find at least inherent support for the step (b) requirement of "sensing the presence of at least one activated cell from said number of memory cells that is erased to a state other than one of at least two data states." Step (5) of instant Figure 23 shows verification that "READ DATA = PROGRAM DATA" for all addressed cells. If there is no verification, the flowchart proceeds to step 6, which denotes applying a pulse of program voltage only to the addressed cells not verified. We find that the artisan would have immediately recognized that -- at least in the case identified by appellants in which

a cell is "programmed slightly" from the "erased" state -- there is necessarily a sensing that a cell is in an erased state. When the "read data" is not the same as the "program data," then the cell is in an erased state. In that event, the process flows to step (6) in Figure 23 for applying program voltage to cells not verified.[3]

We thus do not sustain the rejection under 35 U.S.C. § 112, first paragraph, for lack of written description support. To the extent the rejection may be based on the enablement requirement of the statute, neither do we sustain the rejection on that basis. The rejection does not consider and weigh the relevant factors that may lead to a conclusion of nonenablement. See In re Wands, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988).

[3] Although drawings may provide "written description" support required by 35 U.S.C. § 112, first paragraph (see Vas-Cath, 935 F.2d at 1566, 19 USPQ2d at 1119), we refer to the drawings only for convenience. The algorithm is also described at pages 23 and 24 of the preliminary amendment.

CONCLUSION

The rejection of claims 63-67 under 35 U.S.C. § 112, first paragraph is reversed.

REVERSED

JOSEPH F. RUGGIERO
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

) BOARD OF PATENT
) APPEALS
) AND
) INTERFERENCES

Appeal No. 2001-1272
Application No. 09/056,398

SKJERVEN MORRILL LLP
THREE EMBARCADERO CENTER, 28TH FLOOR
SAN FRANCISCO , CA 94111

U.S. INTERNATIONAL TRADE COMMISSION,

INVESTIGATION NO. 337-TA-382

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of)
)
CERTAIN FLASH MEMORY CIRCUITS) Investigation No. 337-TA-382
AND PRODUCTS-CONTAINING SAME)
)

INITIAL DETERMINATION
Administrative Law Judge Sidney Harris

APPEARANCES:

For Complainant SanDisk Corporation:

Michael A. Ladra, Esq.
Kenneth B. Wilson, Esq.
Robert Moll, Esq.
Monica Mucchetti, Esq.
James C. Yoon, Esq.
Lisa G. Meckfessel, Esq.
Wilson, Sonsini, Goodrich and Rosati
650 Page Mill Road
Palo Alto, California 94304-1050

Christopher T. Lutz, Esq.
Jonathan A. Gluck, Esq.
Steptoe and Johnson
1330 Connecticut Avenue, N.W.
Washington, D.C. 20036-1795

For Respondents Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc.:

Robert F. Ruyak, Esq.
Cecilia H. Gonzalez, Esq.
Thomas J. Scott, Jr., Esq.
Robert A. Auchter, Esq.
Bert C. Reiser, Esq.
John W. Bohn, Esq.
Howery & Simon
1299 Pennsylvania Avenue, N.W.
Washington, D.C. 20004

For the Office of Unfair Import Investigations of the United States nternational Trade Commission:

Juan Cockburn, Esq.
Jeffrey R. Whieldon, Esq.
William F. Heinze, Esq.

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	)	
	)	
CERTAIN FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME	)	Investigation No. 337-TA-382
	)	

INITIAL DETERMINATION
Administrative Law Judge Sidney Harris

Pursuant to the Notice of Investigation, 61 Fed. Reg. 7122-7123 (1996), this is the Administrative Law Judge's Initial Determination in the Matter of Certain Flash Memory Circuits and Products Containing Same, United States International Trade Commission Investigation No. 337-TA-382. 19 C.F.R. § 210.42(a).

The Administrative Law Judge hereby determines that a violation of section 337 of the Tariff Act of 1930, as amended, has been found in the importation and the sale within the United States after importation of certain flash memory circuits and products containing same by reason of infringement of claims 1, 2 and 4 of U.S. Letters Patent 5,418,752 and claim 27 of U.S. Letters Patent 5,172,338.

TABLE OF CONTENTS

C. Claim 27 of the `338 Patent

Claim 27 of the `338 patent is as follows:

> In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:
>
> means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and
>
> means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

CX 2 at col. 26, lines 28-54.

Portions of the claim's lengthy preamble and the additional claim elements are at issue. According to Complainant a key feature of the claim 27 invention is allowing the programming of a chunk of cells in parallel, but treating each cell as if it were programmed individually for purposes of verification and inhibiting further programming of verified cells. Harari, Tr. 261-264 The preferred embodiment of claim 27 of the `338 patent describes a multi-state rather than a binary semiconductor device. The claim, however is not limited to the multi-state device. See e.g., CX 2 at col. 11, lines 56-61. Each of the portions of claim 27 which are in controversy will be

discussed below.

1. The Erase Electrode Element

The preamble of claim 27 recites as one of its elements "an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell."

The term "erase electrode" is found in the '338 patent only in the claims.[34] CX 2. The term "electrode" is commonly understood in the semiconductor industry as a terminal to which an electrical signal is applied to perform some function. Pathak, Tr. 792, 918. An "erase electrode" is understood in the semiconductor industry as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. Pathak, Tr. 792. Thus, because the term "erase electrode" is not defined in the '338 patent as having anything other than its ordinary meaning, it is properly construed in the context of claim 27 as any terminal in a flash memory device to which erase voltage conditions are applied to draw electrons off the floating gate.

Respondents do not expressly contest this definition of "erase electrode" but argue that as used in the '338 patent, the term requires a separate structure for each cell which is dedicated specifically to drawing electrons off the floating gate. See, e.g., Respondents' Post-Hearing Br. at 20-21. Neither Complainant nor OUII adequately support this argument concerning the erase electrode.

Although the erase gate is used in the preferred embodiment as an erase electrode, various structures or terminals in a flash memory device can also

---

[34] See CPFF 257; SPFF 98.

function as an erase electrode as that term would be commonly understood, including the silicon substrate. Harari, Tr. 77-83. Indeed, the record shows that various companies (which are not parties to this investigation) have used the substrate instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. Harari, Tr. 77-83; CPX 25.

Respondents further argue that the silicon substrate cannot serve as an erase electrode in its devices because claim 27 requires that the erase electrode be "receptive to specific voltage conditions for reading, programming and erasing of data in the cell," and that [

[C]

] Respondents' Post-Hearing Br. at 21. As addressed below in the section on the infringement issue, it is found that at least certain of respondents devices satisfy this claim element.

2. The Increment/Decrement Element

The preamble of claim 27 imposes the limitation that the memory cell have "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions."

All of the devices at issue in this investigation (Samsung and SanDisk devices) are binary devices.[35] Complainant argues that for a binary device,

[35] As discussed in the Background section of this Initial Determination, "multi-state" -- or "multi-level" -- devices are not currently in commercial use. See FF 30.

this element of claim 27 should be interpreted to cover a cell that achieves the programmed state by increment of the charge level with successive applications of programming voltage conditions, or a cell that achieves the erased state by decrement of the charge level with successive applications of erasing voltage conditions (or a cell that can perform both of these functions).

Respondents argue that the portion of claim 27 at issue includes two limitations: one requiring the successive application of voltage conditions to program (by putting charge on the floating gate) and the other requiring the successive application of voltage conditions to erase (by removing charge from the floating gate). They argue that "without the term 'or' this claim would merely recite counteracting applications of programming and erasing voltage conditions repetitively incrementing and decrementing charge without any net change in the charge level on the floating gate." Respondents' Post-Hearing Br. at 20-21.

OUII takes the position that claim 27 does not require successive applications of both programming voltage conditions and erasing voltage conditions.

Respondents argue that Complainant's interpretation of the word "or" allows for a broader construction of the patent claim than their interpretation. Citing the Federal Circuit's opinion in Athletic Alternatives, Inc. v. Prince Mfg., Inc., 73 F.3d 1573, 1581 (Fed. Cir. 1996), they argue that a court should adopt the narrower of two possible constructions, and that this element of claim 27 should be construed to cover only a device that achieves a specific memory state through successive applications of voltage, during programming and erasing. Respondents' Reply Br. at 10.

In Athletic Alternatives, the Federal Circuit highlighted the fact that patent claims perform the function of putting others on notice of the boundaries of the invention, and held, as follows:

> Where there is an equal choice between a broader and a narrower meaning of a claim, and there is an enabling disclosure that indicates that the applicant is at least entitled to a claim having the narrower meaning, we consider the notice function of the claim to be best served by adopting the narrower meaning.

Id. at 1581.

However, claim 27 of the `338 patent does not present a case of an equal choice between two meanings. The simplest meaning of the claim element at issue is that one may use successive applications of programming voltage conditions or successive applications of erasing voltage conditions in order to practice the claimed invention. The word "or" in this instance serves its normal function of indicating the availability of an alternative or a choice. Webster's at 1585.

Respondents would read an additional limitation into the claim by requiring that in every instance in which one sought to change the charge level of a cell one must make successive applications of programming or erasing voltage conditions. That additional limitation is not required by the language of the claim. Consequently, based on the plain language of the claim, there is not an equal choice to be made.

Furthermore, other evidence found in the specification and adduced at the hearing supports the broader construction of the claim. The increment/decrement element at issue corresponds to the programming algorithm illustrated in Fig. 15 (item 6), which is described in the text at col. 19, line 57 through col. 20, line 16, whereas the erasing algorithm is illustrated separately in Fig. 11 (items 1 and 2), which is described at col. 16, lines

18-25. With respect to both of these algorithms the charge on the floating gate is changed incrementally.

Thus, in the preferred embodiment disclosed in the specification, the patentees provided examples of incremental programming and of incremental erasing. See CX 2 at col. 18, lines 21-29. However, the fact that the preferred embodiment provides an example of each incremental operation does not mean that an additional limitation should be read into claim 27 that requires both incremental operations in all operations covered by the claim. See Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 867 (Fed. Cir. 1985)("Generally, particular limitations or embodiments appearing in the specification will not be read into the claims."); see also E.I. DuPont de Nemours & Co. v. Phillips Petroleum Co., 849 F.2d 1430, 1433 (Fed. Cir.), cert. denied, 488 U.S. 986 (1988)(prohibiting the reading of limitations from the specification into the claims "wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim").

The application of voltage conditions for programing and the application of voltage conditions for erasing are independent of each other. Harari, Tr. 1861, 1870. In both binary and multi-state devices, one may design for incremental programming and/or incremental erasing. However, programming and erasing are not part of the same operation. Harari, Tr. 1869; Pathak, Tr. 937.

Furthermore, in a multi-state device the reason for using incremental erasing is different from the reason for using incremental programming. In a multi-state device, different charge levels should correspond to different data. However, the consequences of over-erasing are endurance-related. The effect of over-erasing is not catastrophic to the performance of the device. Harari, Tr. 1870; Tutorial (Harari) Tr. 75-77; Guterman, Tr. 577-578.

Consequently, given the technical context in which the wording of claim 27 arose, it is proper that the claim be accorded the more ordinary, less complex meaning, such that one may use successive applications of either programming or erasing voltage conditions. It is not required that one use both program and erase incrementally in order to practice the claimed element.

3. **The Temporary Storage Means**

The preamble of claim 27 recites as one of its elements a "means for temporarily storing a chunk of data for programming a plurality of addressed cells." Complainant argues that in the context of this claim, the term "temporarily storing" would be understood by one of ordinary skill and should be interpreted to mean that the data for each cell is stored impermanently, but at least long enough to complete the programming of that cell. OUII argues that "temporarily storing" should be construed to mean storing as long as the individual cell in the chunk continues to receive the programming conditions. However, Respondents argue that "the term `temporarily' must be construed to mean during the entire programming process for the entire chunk of data and not merely until a cell has been verified once." Respondents' Post-Hearing Br. at 22.

The evidence of record shows that in the context of the `338 patent, the term "temporarily storing" would be understood by one of ordinary skill to refer to a period of storage lasting at least as long as but not necessarily longer than the amount of time necessary to verify and terminate programming to the cell to which the stored data relates. After the programming of a cell is completed, the information used to program that cell is not used again. Harari, Tr. 248-249.

In claim 27 the patentees could have simply called for a means of

storing a chunk of data for programming.[36] However, they elected to add the word "temporarily" to the claim language. The term "temporarily" ordinarily means "for a brief period: during a limited time: briefly." Webster's at 2353. Thus, by adding the word "temporarily" the patentees have emphasized the brief nature of the data storage. That tends to support the claim interpretations proposed by Complainant and OUII, rather than Respondents. The brief nature of data storage is confirmed by reference to the specification and other evidence.

The means in question is disclosed in Figure 5, including block 190 (labeled "Read/Program Latches and Shift Registers"). Harari, Tr. 247-249; Thomas, Tr. 1509-1511; CX 2, at col. 19, line 27 through col. 20, line 36. It may be that in the preferred embodiment the data is stored in the latches until verification has occurred for the entire chunk of data stored therein, yet there is no express requirement to that effect. Thomas, Tr. 1510-1511; Pathak, Tr. 939. Moreover, after a particular cell to be programmed is verified, the data stored in the latch 190 serves no function for the cell that is already programmed, while the programming continues for the rest of the chunk. Harari, Tr. 247-249; Mehrotra, Tr. 329; Guterman, Tr. 587-588.

One of ordinary skill in the art knows that once programming and verification has taken place, the job is done for the stored data, and that "temporarily" in that case would mean just until the job is done. Pathak, Tr. 940-944. Thus, this element of claim 27 should not be construed so as to require storage of all data in a chunk until all cells to be programmed in accordance with the chunk of data have been programmed and verified. The data

---

[36] In the context of the '338 patent a "chunk" is "typically several bytes," and may be used to refer to the number of cells required to program the chunk. CX 2 at col. 19, lines 10-12.

need be stored only long enough for the programing and verification of the particular cell.

4. The Parallel Programming Means

The preamble of claim 27 of the `338 patent recites as one of its elements a "means for programming in parallel the stored chunk of data into the plurality of addressed cells." Complainant argues that in the context of claim 27, the phrase "programming in parallel" should be construed as referring to the function of simultaneously programming a plurality of cells, without reference to the manner of programming used. Respondents argue that the parallel programming means is limited to devices that program using a Hot Electron Injection ("HEI") programming process.[37] See Respondents' Post-Hearing Br. at 24.

Figure 14 of the `338 patent discloses certain structures with which the parallel programming function can be performed. CX 2 at col. 5, lines 40-41, col. 19, lines 27-41; Mehrotra, Tr. 330. In particular, Figure 14 shows an embodiment in which a Program Circuit with Inhibit, block 210, performs the parallel programming function, with the source multiplexer (or "mux") 107 and the drain mux 109 providing the data path. CX 2 at col. 19, lines 27-41; Mehrotra, Tr. 330-334. Thus, the parallel programming means should be construed to include these structures or their equivalents.

The cells in the preferred embodiment of the `338 patent are connected in a NOR architecture configuration. Pathak, Tr. 812-813. HEI programming is thus appropriate for use with the cells described in the preferred embodiment. Harari (Tutorial), Tr. 51-52; Mehrotra, Tr. 334-335. However, the language of claim 27 is silent on the cell structure and the corresponding programming

---

[37] HEI as well as the Fowler-Nordheim method of programming are discussed in the Technological Background section. See FF I 17-22.

method that must be used. Indeed, the '338 patent is not a patent on cell architecture such as NOR or NAND, and which programming method should be used with a particular cell structure. The patent merely recites the broad, general function of "programming in parallel" without specifying the programming method. One of ordinary skill in the art would know that parallel programming can be achieved in more than one way depending on the type of cell structure selected in a device. Furthermore, circuit designers are familiar with the various methods of programming cells depending upon their structures. Pathak, Tr. 944-946; Harari, Tr. 1861-1865. Thus, claim 27 should not be construed to require HEI programming.

In claim 27 of the '338 patent, "programming in parallel" means that programming takes place for more than one cell at a time, such that all cells selected for programming in accordance with a chunk of data receive programming conditions at the same time. See Harari, Tr. 76; Pathak, Tr. 807-808; CX 2 at col 19, lines 30-31 ("The EEprom array 60 is addressed by N cells at a time.").

5. The Verifying Means

The preamble of claim 27 recites as one of its elements "means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data."

The record evidence shows that the term "verifying" as it is used in claim 27 of the '338 patent normally would be understood by one of ordinary skill to refer to the process of determining whether the data in a memory cell matches the data that is targeted to be written into the cell.[38] Guterman,

[38] Mr. Thomas, Respondents' expert on whether Complainant SanDisk practices the '338 patent and on whether Samsung infringes the '338 patent, testified that the term "verify" is ordinarily used very loosely in the (continued...)

Tr. 489-490, 499. The `338 patent contains no contrary or inconsistent definition of the term.

However, Respondents point out that the claim language requires that the programmed data be verified "with" the chunk of stored data, and argue that claim 27 must read only on a device that verifies through the use of a comparator, as in the only structure disclosed in the `338 patent specification for verifying.

Questions are therefore raised as to whether claim 27 should be construed to require the use of a comparator, and whether a structure designed for use in a binary device can be equivalent to the structure disclosed in the `338 patent. These are especially pertinent questions because the Samsung and SanDisk devices at issue are binary devices and [[C]

]

In a multi-state device, such as that described in the `338 patent's specification, a cell can be in one of several states. In performing the verification function, the first step is to determine the state of the cell to be verified (e.g., 0, 1, 2, 3). After determining the state the cell is in, the next step is to determine whether the cell is in the target state for that cell. If the cell is in the target state, the cell is verified; if not, further programming is required. Guterman, Tr. 490-493; CPX 46.

In a binary device, before programming can begin all cells must be in the erased state. Guterman, Tr, 493-495; CPX 48. Inasmuch as all cells start in the erased state, if the targeted state of a particular cell is the erased state, then the cell is in the targeted state before the programming cycle

---

[38](...continued)
semiconductor industry to refer to the process of determining whether a cell is finished programming. Thomas, Tr. 1594-1595.

begins, and therefore no further action needs to be taken with respect to that cell. Harari, Tr. 264-265; Guterman, Tr. 493-495, 499-503; CPX 48. If the targeted state of a particular cell is the programmed state, and if the cell is not in the targeted state before the programming cycle begins, then programming pulses must be applied to bring the cell to its targeted state. Guterman, Tr. 493-495; CPX 48. For cells targeted to be in the programmed state, the cell is read after each programming pulse to verify whether the cell is in the programmed state (i.e., reads a "1"). Once the cell is sensed to be in the programmed state, further programming to that cell is terminated. Guterman, Tr. 493-495; CPX 48.

Figure 11-E of the `344 patent (which is incorporated by reference into the `338 patent) discloses circuitry that corresponds to the verify means in a multi-state implementation of the claim 27 invention. Figure 11-E depicts a multi-state implementation for a single cell in which the cell is able to hold one of four states. CX 2 at col. 4, lines 23-30; Guterman, Tr. 498-499; CX 3 (the `344 Patent); CPX 64. Figure 11-E discloses four sense amplifiers, one associated with each of the four states that the cell can hold. Each of the four sense amplifiers senses whether the current passing through the cell is greater or lesser than the reference current corresponding to the state associated with that sense amplifier. In the multi-state embodiment disclosed in Figure 11-E, once the sense amplifiers perform their sensing operation, the results are fed into the comparator disclosed in Figure 11-E, which determines whether the state of the cell matches the targeted state of the cell. Guterman, Tr. 499-503; CX 3, Fig. 11-E.

A binary embodiment equivalent to that disclosed in Figure 11-E of the `344 patent would not require all the circuitry disclosed for a multi-state implementation. Guterman, Tr. 499-503. In a binary device, it is unnecessary

to have more than one sense amplifier to perform the verification function of claim 27, since the only decision or verification that the device has to make is whether the cell is in the programmed state. Guterman, Tr. 499-503; Allen, Tr. 1173; CPX 64, CPX 66. For a binary device, it would be logical for a circuit designer to simplify the structure of Figure 11-E by eliminating three of the four sense amplifiers and the buffers and circuitry uniquely associated with those sense amplifiers, since they serve no function in a binary device and unnecessarily occupy surface area on the chip.[39] Furthermore, with a single sense amplifier, it is unnecessary to have a separate comparator circuit, since that comparator would merely replicate the function of the sense amplifier.[40] Guterman, Tr. 499-503; CPX 64, 66.

Consequently, the structure disclosed in Figure 11-E of the `344 patent could be reduced to a circuit with a single sense amplifier and no comparator for use in a binary device, and such a structure would be the structural equivalent of Figure 11-E. It could also be used to perform the function of verifying that addressed cells are in the correct state.

---

[39] Dr. Allen, Respondents' expert on the issue of patent validity, testified that a device that only verifies whether the cell is in the programmed state would satisfy the verify means of claim 27. As discussed further below in the section on patent validity, Dr. Allen testified that the "means for verifying" element of claim 27 is satisfied by the M293, a binary device that, like the SanDisk and Samsung flash memory devices, performs the verification function using a single sense amplifier (without a separate comparator circuit) to ascertain whether cells targeted to be programmed have reached the programmed state, while ignoring the cells targeted to remain in the erased state. See Allen, Tr. 1178-1180.

[40] The `344 patent expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (which could indicated "programmed") and "0" (for "erased"). CX 3 at col. 26, lines 55-60. In fact, the `344 patent teaches that in a four-state storage device the comparison may be accomplished with four consecutive read cycles and only one sense amplifier, with a different reference applied at each cycle, if the additional time required for reading is not a concern. CX 3 at col. 25, line 64 through col. 26, line 17.

Figure 16 of the `338 patent discloses certain additional structures for performing the verification function in a multi-state device. In the circuit compare module 703 shown in the Figure, the read bits are compared bit by bit with corresponding program data bits, i.e., it is determined whether there is a match between the read and write data.[41] This is performed by XOR (exclusive OR) gates such as 711, 713 and 715 shown in Fig. 16. The specification states that the number of such XOR gates used depends upon the number of binary bits encoded for each cell. The output of the XOR gates passes through a NOR gate 717 whenever all the bits are verified, and node 726 is taken high so that latch 721 is set in the verified state. Once latch 721 is set, the cell is inhibited from further programming during subsequent programming pulses that may be applied on the chunk. If, however, the read data does not match the write data, then latch 721 remains in its previous state.[42] Mehrotra, Tr. 339-340; CX 2 at col. 20, lines 17-51.

The Figure 16 multi-state embodiment could be modified for a binary device by making some simplifications to the structures that would be obvious to an ordinary flash memory circuit designer. Mehrotra, Tr. 342; Pathak, Tr. 819-820.

In fact, the `338 patent contemplates an embodiment with only two states. The `338 patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at

---

[41] In the preferred embodiment, "[C]ircuit 200 comprises N cell compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col 20, lines 18-20.

[42] Figure 5 also provides a general identification of a "Compare Circuit", block 200, that performs the verify function in one embodiment of claim 27. The Program Circuit with Inhibit disclosed in block 210 of Figure 5 of the `338 Patent performs the function of inhibiting further programming by removing high voltage from the drain of the cell to be inhibited. Guterman, Tr. 508-510; Harari, Tr. 258, 267-269.

least K - 1, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed ...." CX 2 at col. 11, lines 56-61. In other words, in the case of a two-state device, only a single reference level need be used for performing the verification function (e.g., where "0" equals the programmed state, the device only needs to determine whether the cell has reached the "0" state, and can ignore cells targeted to remain in the erased state).

It would be obvious to a circuit designer of ordinary skill to eliminate all but one of the XOR gates (711, 713, 715) in a binary device, since only one bit is being stored in the cell (i.e., "L" = 1). Mehrotra, 342-343; CPX 120; Pathak, Tr. 820-822; CPX 122. In a binary device, it would be obvious to a circuit designer of ordinary skill to change NOR gate 717 to a single inverter, since there would only be a single XOR gate, and therefore only a single input. Mehrotra, Tr. 342-345; CPX 120; Pathak, Tr. 820-822; CPX 122.

Furthermore, in implementing Figure 16 of the '338 patent in a binary device, the possible combinations of read (R) and write (W) are greatly reduced, as compared to a multi-state device, such that it is not necessary to implement the logic inherent in XOR (exclusive OR) gates and NOR gates to verify a cell.[43] Thus, one would expect to make additional simplifications to the circuitry shown in Figure 16 by eliminating entirely the XOR gates and the NOR gate 717. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128. It would be logical to simplify the verification and

[43] There are only four logically possible states: R=0 and W=0; R=0 and W=1; R=1 and W=0; R=1 and W=1. For example, in the first scenario (R=0 and W=0), the data read from the memory is zero (erased) and the data desired to be written into the memory is also zero. Note also that the third scenario (R=1 and W=0) should not be possible because all cells are required to be in an erased state before programming starts. Mehrotra, Tr. 345-346.

inhibit circuitry disclosed in Figure 16 to consist merely of R (where R is the output of the sense amplifier) and the data latch 721, as shown in CPX 127. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128. One familiar with the differences between multi-state cells and binary cells would simplify the verify and inhibit circuitry shown in Figure 16 to the circuitry shown in CPX 127, because such a simplification would reduce the size of the chip, reduce the logic, reduce costs, and give more efficient operation. Pathak, Tr. 829-829.

Based upon the language of claim 27, the specifications of the `338 and `344 patents, as well as extrinsic evidence adduced at the hearing, claim 27 is properly construed to cover a binary device that uses a single sense amplifier to verify whether a cell has reached its programmed state. Furthermore, it would not be logical to construe claim 27 to require the use of a comparator in a binary device. Accordingly, the claim 27 verification means should be interpreted to include the binary simplifications discussed above.

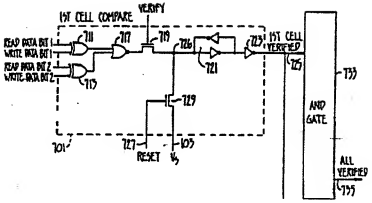
6. The Inhibiting Means

Claim 27 of the `338 patent recites as one of its elements "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells."

Figure 16 of the `338 patent discloses one embodiment of the compare circuit used in the multi-state, preferred embodiment. Figure 16 also discloses circuitry that inhibits further programming of the memory cells. CX 2 at col. 20, line 17-18; Mehrotra, Tr. 340.

The pertinent circuitry is depicted in Figure 16 of the `338 as

follows:[44]



In the circuit shown in Figure 16, a latch 721 performs the function of inhibiting further programming to correctly verified cells. Mehrotra, Tr. 340-342. When a cell is correctly verified, the result is sent to latch 721, which is then set to the verified state. Mehrotra, Tr. 340; CX 2 at col. 20, lines 28-32. The specification mentions that at the end of a programming pulse all the latches are reset to the unverified state. Node 726 can only be reset by transistor 729 and not by node 717 after node 726 goes high. Mehrotra, Tr. 3. Once latch 721 is set in the verified state, the cell is inhibited from further programming during any subsequent programming pulses which may be applied.[45] Mehrotra, Tr. 340.

---

[44] The illustration, supra, like the illustration contained in Respondents' Reply brief, depicts the circuitry of one compare module contained in the preferred embodiment (compare module 701). Figure 16 and the text of the specification provide for "N compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col. 20, lines 18-20, Fig. 16.

[45] The `338 patent specification teaches that "[p]rogramming and verification are repeated until all the cells are correctly verified in FIG. 15(7)." CX 2 at col. 20, lines 14-16. Thus, each cell must be read to

(continued...)

Thus, latch 721 in Figure 16 is a "one-way latch." Latches are often referred to as "one-way" or "two way." One-way latches and two-way latches are often drawn in the same manner. Mehrotra, Tr. 372, 397. Yet, they function differently. A two-way latch freely switches back and forth between two states when different input values are applied. Thus, if the input to the latch is a 0, then the value saved in the latch becomes a 0. If a subsequent input is a 1, the latch then saves a 1. Allen, Tr. 1077. However, a one-way latch is said to move in only one direction. Thus, for example in Figure 16, when verification occurs and the latch is set to a 1, the latch does not go back to a zero during the overall cycle of iterations. See Allen Tr. 1078 (for the way a one-way latch works). Thus, a one-way latch like that used in Figure 16 of the `338 patent will not allow the detection of so-called "program disturb conditions" where, due to defects in a part, a cell goes back to an erased state before the entire chunk of data is verified. Nor will a one-way latch allow the detection of conditions in which a part fails and a cell is disturbed from an erase into a programmed state. Harari, Tr. 250-252; Mehrotra Tr. 374-378; CX 2. Furthermore, neither claim 27 of the `338 patent, nor the specification mentions the detection of program disturb conditions.[46]

---

[45](...continued)
determine whether the read and write data for that cell match.

[46] Respondents state that Dr. Harari admitted that a device that verifies on an iteration basis would be within the scope of claim 27. See RPRFF 281 citing Harari, Tr. 270. Dr. Harari made the following statement during cross-examination in response to a hypothetical question:

> Q. Well, let me ask you this. If -- if the Samsung device continued to verify, even if it was useless, would you say that it was outside the scope of this claim?
>
> A. No, of course not.

Harari, Tr. 270.

(continued...)

CX 2.

With respect to Figure 16, the specification teaches that the output of the XOR gates passes through NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the bits are verified, otherwise a "0" appears there. When verification occurs (i.e. "[w]hen the control signal VERIFY is true"), "this result is latched to latch 721 such that the same result at the output of NOR gate 717 is also available at the cell compare module's output 725." CX 2 at col. 20, lines 25-32 (emphasis added). The output 725 is fed through an output line to the "program circuit with inhibit 210 of FIG. 5."[47] CX 2 at col. 20, lines 33-36.

The specification in describing the functions of latch 721 states that "[w]hen the control signal VERIFY is true, this result is latched to latch 721." It says nothing about setting latch 721 in case of a subsequent (or previous) control signal VERIFY that is not true. Thus, the specification does not provide that it will return to an unverified state during the program

---

"(...continued)
It is not clear what type of circuitry was assumed by the questioner or what type of circuitry Dr. Harari had in mind when he responded. It is significant that Dr. Harari was asked about a device that somehow continued to "verify, even though it was useless," not about a circuit that continued to apply programming conditions. Claim 27 requires an inhibition against further programming, not further, useless verification. The hypothetical circuit in question did not exclude the fact that it would have an operational program inhibit as required by claim 27.

[47] The program circuit is the circuit that removes voltage from a cell so that further programming (or over-programing) cannot take place. However, as described in the specification, the program circuit depends upon the data latched by latch 721. Although latch 721 is physically contained within the compare module in the preferred embodiment, the results of the comparison of read and write data are latched to latch 721. Latch 721 does not perform that comparison. It plays a role in making sure that correct output is available from the compare module for input to the program circuit.

and verification of a chunk of data."[" Indeed, since latch 721 is a one-way latch, once the latch is set, the stored data cannot be affected by the output of NOR gate 717. Mehrotra, Tr. 340-341.

The preferred embodiment of the '338 patent is a multi-state device. If latch 721 were not a one-way latch, there would be catastrophic failure of the multi-state device. See McGreivy, Tr. at 1697-1701, 1797-1799; CX 2 at col. 19, lines 4-26. The specification provides that in order to change the setting of latch 721:

> At power-up or at the end of program/verify of a chunk of data, all cell compare module's outputs such as 725, 727 are reset to the "not verified" state of "0". This is achieved by pulling the node 726 to V_{ss} (0 V) by means of the RESET signal in line 727 to a transistor 729.

CX 2, col. 20, lines 46-51.

Thus, the specification teaches that latch 721 must be reset at power up, as well as at the end of each program/verify of a chunk of data. The '338 patent also teaches that before any programming occurs, a read operation must

---

[" Respondents' expert, Dr. Allen, testified at the hearing that latch 721 is a two-way latch. His opinion appears to be based in part on an incorrect reading of the specification text. Referring to column 20, starting at line 28, he testified as follows:

> So we're pointing out that indeed in the language of the specification, the specification calls for on any given iteration within the overall cycle, whatever value is read out on the NOR gate 717 is to be brought over here to the node 725. The only way for that to happen consistently on every iteration as indicated by the language I just read, is for latch 721 to be able to go back and forth. That is to be a two-way latch.

Allen, Tr. 1086 (emphasis added).

However, the specification does not state that whatever value is read out on NOR gate 717 is to be brought over to node 725. As discussed, supra, the specification states in column 20 that the output of NOR gate 717 is available at the cell compare module's output 725 only when the control signal VERIFY is true.

be performed to verify that the read data and the write data match. Thus, if latch 721 were a two-way latch, before the commencement of programming a cell would be read and if found not to be in the correct state, latch 721 would flip back to the not verified state in response to the output of NOR gate 717. A reset operation such as that disclosed in the specification would not be required. Mehrotra, Tr. 399-400. Instead, the specification shows that latch 721 can only be reset by the effect of transistor 729. See Mehrotra, Tr. 342. The specification demonstrates that latch 721, once set to the verified state, remains in the verified state during the entire program/verify of a chunk of data. Then, latch 721 is returned to the "not-verified" state by a reset operation in which node 726 is pulled down, as one would expect in the case of a one-way latch.[49] See Mehrotra, Tr. 400; Allen, Tr. 1079, 1086.

In addition to the disclosure of Figure 16, including latch 721, Figure 5 of the `338 patent contains a block 210 entitled "Program Circuit with Inhibit." This block provides no detail regarding the specific circuitry that actually inhibits further programming. CX 2; Guterman, Tr. 508-510. Figure 17 shows "one embodiment of the program circuit with inhibit 210 of Fig. 5 in more detail." CX 2 at col. lines 52-53. The one embodiment shown in Figure 17 is relevant to the Hot Electron Injection programming method used in the preferred embodiment. The circuitry in Figure 17 is for removing voltage from the drain of a cell to inhibit further programming. CX 2 at col. 20, line 52 through col. 21, line 8; Mehrotra, Tr. 352-353; Guterman, Tr. 511-513. Respondents argue that the means for inhibiting further programming of

---

[49] In order to pull down latch 721, one would have to design the circuit shown in Figure 16 to have transistors of the proper size. Allen, Tr. 1079; Mehrotra, Tr. 409. The `338 patent does not indicate the size of the transistors involved in Figure 16. Nonetheless, one of ordinary skill would know how to size the transistors shown in Figure 16 relative to the size of NOR gate 717 so as to achieve a one-way latch. CX 2; Mehrotra Tr. 404-409.

correctly verified cells among the plurality of addressed cells is the program circuit disclosed in Figure 17 of the '338 patent. Respondents' argument with respect to the inhibit means is linked to their argument that HEI programming and a cell that uses such programming must be used in the claimed invention. See Respondents' Post-Hearing Br. at 26-27, RPFF 463-465. This argument has been rejected above in the discussion of the parallel programming means. Furthermore, although the circuitry disclosed in Figure 17 is part of one way of implementing the claimed invention, it depends upon circuity that is actually located with the "compare modules," e.g., latch 721 and compare circuit module output 725.

To one skilled in the art, one way of implementing the inhibit means is to combine certain disclosures in Figures 16 and 5, in particular block 190 of Figure 5, which is entitled "Read/Program Latches and Shift Register." The temporary storage latch disclosed in block 190 of Figure 5 can also serve as the inhibit latch 721 of Figure 16 of the '338 patent. Mehrotra, Tr. 349-351; CPX 120; CX 2, Fig. 16; Pathak, Tr. 835-839; CPX 57C-58C; CPX 124-125. A flash memory designer of ordinary skill would seek to combine the functions of the temporary storage latch and the verify inhibit latch in a single structure in order to save transistors, thereby reducing the surface area of the chip. Pathak, Tr. 839-840.

Consequently, the inhibit means should be interpreted to include a one-way latch 721 or its equivalent.

7. **The Final Means Plus Function Element**

Claim 27 recites as its final element "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly."

Complainant argues that this element refers to an iterative process in which the cells are repeatedly verified, utilizing additional programming pulses until all of the addressed cells have been verified. The claimed uniqueness of complainants invention is that the successive programming pulses are applied to only those cells which have not yet been correctly verified (i.e. have not reached their desired state at which point all further programming to already verified cells is permanently inhibited through the remainder of the program cycle).[50]

Respondents argue, however, that Complainant would interpret claim 27 to place an additional "permanently inhibit" limitation on the programming algorithm of the `338 patent. According to Respondents, the `338 device does not permanently inhibit programming of cells that are erroneously verified as correctly programmed. See, e.g., Respondents' Post-Hearing Br. at 14; Respondents' Reply Br. at 12-16.

Figure 16 of the `338 patent discloses structures that correspond to the final means-plus-function element of claim 27 in a multi-state implementation. Those structures include the one-way latch 721, the outputs such as output 725, as well as AND gate 733 whose single output 735 is used to signal the controller in the preferred embodiment that all cells in the chunk of data have been correctly verified. Mehrotra, Tr. 341; CX 2 at col. 20, lines 18-51. Accordingly, the final element of claim 27 should be construed to include these structures or their equivalents.

The parties disagree as to the plain meaning of the patent claim. In particular, there is disagreement as to the effect of the final phrase "until

---

[50] OUII agrees with Complainant that "claim 27 is limited to devices which inhibit programming of correctly verified cells for the period of time until all cells are verified correctly." OUII argues that this feature is enabled by latch 721 in Figure 16. OUII Reply Br. at 17 & n.21.

all the plurality of addressed cells are verified correctly." Given the lack of punctuation in the text of the claim and the ordinary meaning of the words contained in that phrase, it appears that the condition specified therein applies to the entirety of the claim language preceding it within the final element, i.e., to both (1) further programming and verifying and (2) inhibiting programming of correctly verified cells. That appears to be the same position taken by Respondents, at least as regards the grammatical function of the final "until ...." phrase contained in the claim element. See Respondents' Post-Hearing Br. at 9-10; Respondents' Post-Hearing Reply Br. at 12.

The Administrative Law Judge reads this final phrase to refer to the fact that the verification and programming process continues until the entire chunk of data is programmed. However, the fact that the final phrase modifies the entire claim element does not require the meaning for the final element proposed by Respondents. Although the final claim element requires further programming until all cells are correctly verified, that does not mean that once a cell is correctly verified that the device must then verify it again and, more significantly, if found no longer to be in the target state that the inhibition against further programming must be removed and the cell must be reprogrammed. Such a limitation is not contained in claim 27, and to construe claim 27 in that manner would ignore the express requirement that programming be inhibited from cells once correctly verified. To construe claim 27 to require that cells which have been correctly verified must be subject to further programming would also be inconsistent with the proper construction of the previous claim element (the inhibiting means), which as discussed above requires a one-way latch like latch 721 in the preferred embodiment or its equivalent.

Furthermore, the description of the means described in the `338 patent specification requires that the programming of each cell be permanently inhibited upon verification.[51] For example, the specification provides in part: "[a]s soon as the programmed state is verified correctly, programming stops." CX 2 at col 18, lines 24-25. The patent provides further that "parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk that have already been verified correctly." CX 2 at col. 19, lines 13-16. Finally, the patent also provides that "it is preferable to apply programming voltages in repetitive short pulse with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates." CX 2 at col. 9, lines 13-18. Each of the passages clearly indicates that the `338 patent will not apply an additional programming pulse to a cell after it has been verified. See Mehrotra, Tr. 253-254; McGreivy, Tr. 1693-1696.

---

[51] Respondents argue that Figure 15 shows that individual cells may be either programmed or inhibited in any individual pulse. See Respondents' Post-Hearing Br. at 4-5; Respondents' Reply Br. at 12; Thomas, Tr. 1510-1511. Figure 15 is a block diagram that depicts an on-chip program algorithm according to the claimed invention. CX 2 at col 5, lines 42-43, Fig. 5. The algorithm is discussed in the text at col. 19, line 57 through col. 29, line 16. The block at Fig. 15(5) is labeled "Verify Read Data = Program Data For All Addressed Cells." If the answer is "No" the diagram indicates in block 6 that a pulse of program voltage is to be applied only to addressed cells not verified. Respondents interpret this diagram to indicate that each cell must be given an additional programming pulse if upon any verification pulse the cell is found not to be verified correctly. However, Figure 15 cannot be read in isolation. It is given clarity by Figure 16, whose latch 721 operates throughout the programming of a chunk of data to identify a cell as correctly verified once it has reached a programmed state. Thus, a cell once correctly verified will be read as such each time the program algorithm reaches the stage depicted in Fig. 15(5), and in accordance with block (6) such a cell will not receive a further program pulse. Such a cell is permanently inhibited from further programming while the remainder of the chunk of data is programmed.

The distinction between conditional inhibition and termination is an important one. As Dr. McGreivy explained, failure to terminate will, over time, overstress a binary device and make a multi-state device malfunction. McGreivy, Tr. 1697-1708, 1793-1813. This point is addressed in the text of the `338 patent, as follows:

> In the prior art EEprom devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller 140 or the CPU 160 for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.
>
> In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue pass [sic] [past] the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEprom chip and the controller, and program verification speed is greatly enhanced.

CX 2 at col. 19, lines 4-26.

Based upon the plain language of claim 27, the discussion of this issue in the specification, and the disclosure of the one-way latch 721, claim 27 is properly construed to include the limitation of termination or permanent inhibit of programming once a cell has been correctly verified.

B. The '338 Patent

Samsung's on-sale bar, anticipation and obviousness affirmative defenses against claim 27 of the '338 patent depend on its argument that the claim covers EEprom devices that inhibit the programing of correctly verified cells for only one iteration. As discussed in detail above, Samsung's proposed construction of claim 27 has not been adopted. It has been found as a matter of law that claim 27 requires permanent inhibition of further programming pulses to a cell that has been verified during the programming of a chunk of data. Consequently, Samsung has not in connection with its affirmative defenses established by clear and convincing evidence that claim 27 of the '338 patent is invalid.

1. On-Sale Bar

Respondents argue that a television tuner manufactured by SGS Thomson, and identified as the M293 device, anticipates claim 27 of the '338 patent, and acts as an on-sale bar under 35 U.S.C. § 102(b), thereby making claim 27 invalid.[46] Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the claim is invalid.

In order to establish an on-sale bar, the Samsung Respondents have the burden of demonstrating by clear and convincing evidence that each element of claim 27 is embodied in the M293 device. See Ferag AG v. Quipp, Inc., 45 F.3d

---

[45](...continued)
'752 is not deficient in that regard. However, Respondents did not raise this issue in their briefs, and the issue is therefore abandoned. See OUII's Reply Br. at 14 n.18.

[46] Under 35 U.S.C. § 102(b), "[a] person shall be entitled to a patent unless the invention was . . . in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States."

1562, 1566 (Fed. Cir.), cert. denied, 116 S.Ct. 71 (1995).[69] However, the evidence of record shows that the M293 device does not perform the claimed function of permanently inhibiting the programming of correctly verified cells "until all the plurality of addressed cells are verified correctly" and therefore cannot act as an "on-sale bar" under 35 U.S.C. § 102(b).

Exemplars of the M293 device were the subject of testing performed during the course of this investigation in order to determine whether the device embodies each of the elements of claim 27 of the '338 patent. Particular emphasis was placed on the device's ability to inhibit programming pulses to correctly verified cells. The testing performed on behalf of Respondents is reflected in the TAEUS Report (RX 180C). SanDisk performed its in-house tests and submitted a Report (CX 199). Testing that was agreed to by both SanDisk and Samsung is reflected in the Chipworks Report (CX 204). Although TAEUS, SanDisk and Chipworks used different testing protocols and conditions, each demonstrated that the M293 device is not capable of permanently inhibiting programming of correctly verified cells as required by claim 27 of the '338 patent.

The TAEUS Report submitted by Samsung shows that the circuitry of the M293 device lacks any structure capable of permanently inhibiting the correctly verified cells from further programming. FF IV 101-102. The M293 test Report submitted by SanDisk, as testified to by Mr. Mehrotra of SanDisk, establishes that the M293 device does not perform the function of permanently inhibiting the programming of verified cells until all the plurality of addressed cells are verified correctly, and does not have the structure to do so. FF IV 98-102. Furthermore, the Chipworks Report also shows that the M293

[69] SanDisk does not dispute that the SGS device was on sale in the United States more than one year before the '338 patent application was filed.

device does not permanently inhibit the correctly verified cells from further programming, or contain circuitry necessary to meet that claim limitation. FF IV 123, 133, 140.

The most significant differences between the M293 device and the structure and the function required by claim 27 are due to the fact that the verification and inhibiting circuitry of the M293 does not include a "one-way" latch that terminates the programming of a cell upon verification. See FF IV 102. Consequently, unlike the invention claimed in the '338 patent, the M293 device only inhibits verified cells on a temporary or conditional basis. FF IV 101.

For example, if a particular bit verifies as programmed after the third programming pulse in the M293 device, it will be inhibited from programming on the fourth pulse. However, since each cell is reverified after each subsequent programming pulse, if the cell should then fail the verification step following the seventh programming operation (e.g., because it was a borderline pass or because an error occurred in the read/verify step), the cell will then receive an additional programming charge during the eighth programming pulse. Gross, Tr. 1453-1454. Thus, the M293 device does not inhibit "programming of correctly verified cells until all the plurality of addressed cells are verified correctly." See FF IV 99.

In addition to proposing a different interpretation for claim 27, Samsung argues that the M293 performs the claimed function of terminating the programming of verified cells because in "normal operation" the device will not apply an additional programming pulse to a cell that has been already verified.

Samsung contends that the additional programming pulses issued to already verified cells during Chipworks testing of the M293 device is

attributable solely to variations in the input voltage and the capacitive loading of the equipment. However, Chipworks concluded that this could not be the case for at least certain of the wave forms generated during testing. See FF IV 145-152.

Furthermore, the purpose of the permanent inhibit function of the `338 patent is to prevent the application of a programming pulse to a cell in those situations where the device experiences a misread or false verify.[70] See McGreivy, Tr. 1697-1708; section on claim construction. Thus, Samsung's argument concerning supposedly normal operations of the M293 does not show that the device contains all the elements of claim 27 of the `338 patent.

Therefore, for the reasons stated above, sales of the SGS M293 device did not act as an on-sale bar to the patentability of claim 27 of the `338 patent.

2. Anticipation (the Torelli Article)

Respondents argue that an article by Guido Torelli, et al., entitled "An Improved Method for Programming a Word-Erasable EEPROM" (the "Torelli Article")((RX 71) anticipates claim 27 of the `338 patent, thereby making the claim invalid.[71] See FF IV 153. The Torelli Article describes the operation and characteristics of the M293 device. FF IV 154. Complainant and OUII take

---

[70] Such occurrences take place under normal conditions without the presence of any testing equipment. See Allen, Tr. 1177.

[71] Respondents' arguments concerning alleged anticipation by the Torelli Article are based on Section 102(b) of the Patent Act, which provides that a person is not entitled to a patent if:

> the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States ....

35 U.S.C. § 102(b).

the position that Respondents have not shown by clear and convincing evidence that the claim is invalid.[72]

In order for the Torelli Article to anticipate claim 27 of the `338 patent, it must be proven by clear and convincing evidence that "all of the elements and limitations of the claim are found within [this] single prior art reference." Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1577 (Fed. Cir. 1991).[73]

As in the case of the M293 device, the Torelli Article does not disclose the function of permanently inhibiting the programming of verified cells. FF IV 154-160. Figure 4 of the Torelli Article and its associated text show that all the cells being programmed are "read/verified" between each and every programming pulse. FF IV 157-158.[74] At trial, all the witnesses uniformly agreed that the M293 device discussed in the Torelli Article does not perform the claimed function of permanently inhibiting the programming of correctly verified cells. FF IV 154-155, 99-102, 151-160. Indeed, there is no structure disclosed or suggested in the Torelli Article, such as a one-way

---

[72] Prior to the hearing, the Administrative Law Judge was informed that Complainant and Respondents sought reexamination of the `338 patent in light of the Torelli Article, and SGS brochures and technical notes. The Administrative Law Judge did not believe it suitable to suspend this investigation based on the particular circumstances existing in this case, including: the fact that the hearing was imminent and the parties had virtually completed preparations for the hearing; the lack of detailed statements from the PTO concerning the effect of the Torelli Article or other references on the `338 patent; and the likelihood of a substantial period of time before a definitive decision would be made by the PTO.

[73] It was not disputed that the Torelli Article was published early enough so that it could be cited against the `338 patent under section 102(b).

[74] In fact, the related M293 device will apply a programming pulse to a cell whenever that cell is read by the device to be in the unprogrammed state regardless of whether it was verified and inhibited during the application of a previous programming pulse. FF IV 154-155, 159-160, 165.

latch, to track whether a cell was verified/inhibited during the application of a previous pulse so as to disable any further programming of that cell. FF IV 159-160.

In addition to the dispositive absence of the termination function, it has not been established that the Torelli Article contains sufficient disclosures of structures required to perform other functions required by claim 27.

The Torelli Article does not disclose any structure for temporarily storing a chunk of data for programming a plurality of addressed cells. FF IV 161. Although one may infer that there is a location for temporarily storing data, it is not clear from the article whether temporarily stored data is to be stored on or off chip. FF IV 162; McGreivy, Tr. 1759-1763.

The Torelli Article does not disclose any structure for verifying the programmed data in each of the plurality of addressed cells with a chunk of stored data. Without further disclosure in the article, one of ordinary skill in the art would not know the type of structure to use for the verification function. FF IV 166.

Finally, the Torelli Article does not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of verified cells until all the plurality of addressed cells are verified. The article does not disclose the type of verification and program inhibit functions required by claim 27 of the `338 patent, let alone a means for continuing such functions until all the plurality of addressed cells are verified. See FF IV 165, 166.

Aside from the failure by the Torelli Article to disclose these elements required by claim 27 of the `338 patent, the insufficiency of disclosure would also deny an individual of ordinary skill the ability to build the device

disclosed in claim 27 of the `338 patent. FF IV 159-166. Consequently, the lack of enablement by the Torelli Article prevents it from anticipating claim 27 of the `338 patent, independently of its failure to disclose the program inhibit element. See Akzo N.V. v. United States Int'l Trade Comm'n, 808 F.2d 1471, 1479 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987) (in order to anticipate a claimed invention, a prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public).

Given the total absence in the Torelli Article of key structures and limitations required by the patent claim, it has not been shown by clear and convincing evidence that the Torelli Article anticipates claim 27 of the `338 patent.

3. Obviousness

Respondents argue that the Torelli article and the devices and product literature (SGS data books and technical notes) based on it render the claimed invention of the `338 patent obvious under 35 U.S.C. § 103, and therefore invalid.[75] Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the `338 patent is invalid.

In order to prove obviousness, it must be demonstrated by clear and convincing evidence that the invention of claim 27 would have been obvious in light of the combined teachings of items of prior art relied on by Respondents. See Graham v. John Deere, 383 U.S. at 37; Jones, 727 F.2d 1524, 1530-32 (Fed. Cir. 1984); Litton, 97 F.3d at 1566 (section 103 obviousness analysis requires a determination of the scope and content of the prior art, the differences between the prior art references and the claimed invention and the secondary indicia of nonobviousness). In addition, it must be shown that

[75] Section 103 of the Patent Act is quoted above in the portion of this section addressing the `752 patent.

one of ordinary skill would have known to combine these items. See Uniroyal, 837 F.2d at 1050-1051.[76] As discussed below, the requisite showing has not been made to find claim 27 of the '338 patent obvious in view of the prior art.

Neither the Torelli Article, nor the SGS data books, nor SGS technical notes include any disclosure or teaching relating to the concept of permanently inhibiting the programming of verified cells, an essential function of claim 27. FF IV 175-189. Furthermore, Samsung introduced no evidence at trial to show that the permanent inhibition of programming of verified cells would have been obvious to an individual of ordinary skill. FF IV 191. Nor did Samsung offer any testimony to suggest that one would know to combine the cited prior art. FF IV 192.

In fact, Samsung has argued against obviousness by taking the position that the function of permanently inhibiting the programming of correctly verified cells would be irrelevant or meaningless to the operation of binary devices. Thus, Samsung has conceded that an individual of ordinary skill would not recognize the possibility that the endurance and operation of a binary EEprom device could be improved by terminating the programming of correctly verified cells. See also FF IV 198, 199.

There is nothing in the prior art relied on by Samsung to indicate that the programming of a cell should be stopped or terminated upon verification. FF IV 175-189. In fact, the Torelli Article, SGS data books and SGS technical notes suggest the opposite. These documents suggest that all the cells being programmed should be verified after each programming pulse. At most, they

[76] An individual of ordinary skill in the art of flash memory has at least a bachelor's degree in a field such as electrical or computer engineering (or experience equivalent thereto) and at least a few years of work experience with EEproms. FF IV 167-172.

teach that the inhibition of further programming pulses is a conditional event that must occur on a pulse-by-pulse basis. FF IV 155-158. Thus, if the "read" conditions on any given cell changes after a cell has been "verified" (i.e., the device correctly or incorrectly reads that the cell is no longer in the "written" state), the respective disclosed devices apply an additional programming pulse(s) to the previously verified cell. FF IV 154, 100. Such a result is contrary to the requirement of claim 27 that the programming of a verified cell be inhibited or disabled until all the addressed cells have been verified.

Furthermore, it was undisputed at trial that the concept of "permanently inhibiting" or "terminating" the programming of verified cells was not obvious to an individual of ordinary skill in 1989. See FF IV 198-226. The non-obviousness of the permanent inhibit feature is demonstrated by the fact that Toshiba, the original designer of the NAND architecture, did not include a permanent inhibit feature in its original 4Mbit flash memory product despite the fact that it is beneficial to the NAND device. FF IV 199, 226.

Consequently, none of the prior art cited by Samsung can individually or in combination invalidate claim 27 of the `338 patent.

The validity of the `338 patent, including claim 27, is further supported by secondary indicia of validity. The `338 patent has been and will be crucial to SanDisk's success in the mass storage flash memory market. FF IV 200. As of 1994, SanDisk was the worldwide leader in the mass storage flash memory with approximately a 40% market share. FF IV 203. Furthermore, Intel, the world's largest commodity flash memory producer, has entered into a licensing agreement for all of SanDisk's patents, including the `752 and `338 patents. FF IV 201.

The Administrative Law Judge finds that it has not been shown by clear and convincing evidence that claim 27 of the `338 patent is invalid due to obviousness.

c. **Claim 27 of the `338 Patent Is Infringed**

Complainant SanDisk takes the position that Samsung's devices practice each of the elements of claim 27, including the seven disputed elements covered in the section of this Initial Determination on claim construction, and that therefore Samsung infringes claim 27 literally or, in the alternative, under the doctrine of equivalents.

The Samsung respondents take the position that their devices do not practice at least six of the disputed claim elements, and that therefore their devices do not infringe claim 27 either literally or under the doctrine of equivalents. Respondents' Post-Hearing Br. at 17.

OUII takes that position that the Samsung devices do not practice all of the disputed elements of claim 27, and that therefore the devices are not infringing.

Samsung's Flash EEprom products are binary devices. As discussed above in the section on claim construction, although the preferred embodiment of the `338 patent is a multi-state device, the specification states that the claimed invention may be applied to a binary device. Indeed, claim 27 reads on a binary device. However, Samsung argues that because of prosecution history estoppel, a binary device cannot be found to infringe claim 27. SanDisk and OUII oppose Samsung on this point.

Before examining each of the individual elements of claim 27, the question of prosecution history estoppel is addressed as a threshold matter.

Samsung argues that during the prosecution of the `338 patent, SanDisk distinguished claim 27 over U.S. Patent No. 4,460,982 to Gee et al. on the basis that the `982 Gee patent would work only for binary memory cells, not multistate cells covered by the `338 patent, and further that SanDisk is estopped from now asserting that binary devices infringe the asserted claims

under the doctrine of equivalents.

In order to distinguish claim 27 of the '338 patent over the prior art, particularly Gee et al., the applicants' agent represented, as follows:

> Claim 27-28 has [sic] been amended to recite inhibiting of further programming of correctly verified cells rather than selective programming of unverified cells.
>
> Gee et al. disclose a programming system operating in parallel on 8 bits of addressed cells. If bits 2, 5 and 7 are to be programmed to the "0" state, programming pulses will be applied to all three cells as long as one of these cells are not verified correctly. This scheme does not work for memory cells having more than two states since some cells will reached [sic] their desired state earlier than others and will continue to pass [sic] the desired state if not stopped.
>
> Thus, Giebel and Gee et al., individually or in combination do not teach or suggest a programming system with means for inhibiting further programming of correctly verified cells among the plurality of addressed cells. It is believed amended claims 27-28 along with amended claim 33 are allowable.

CX 8 ('338 Prosecution History) at SD008951 (emphasis added).

The statements quoted above, and relied on by Respondents (see RPFF 373), say nothing about binary devices. The applicants, through their agent, indicated to the Examiner that their invention, as claimed in claims 27-28 and 33, is suitable for multistate devices because of its ability to inhibit further programming of correctly verified cells, whereas Gee et al. is unsuitable for multistate devices. However, the statements made to the Examiner do not preclude the claim from covering binary devices. These statements pointing out the advantages of the claimed invention with respect to multistate devices do not indicate that the claimed invention and that of Gee et al. operate in the same manner with respect to binary devices. Indeed, the inhibiting of further programming of verified cells occurs regardless of whether the invention of claim 27 is used in a binary device or a multistate

device. As discussed above in connection with claim construction, it is also useful to prevent unnecessary programming in both binary and multistate devices.

Therefore, the Administrative Law Judge finds that prosecution history estoppel does not apply in the case of the `338 patent to prevent claim 27 from covering binary devices such as Samsung's flash EEprom products.

Consequently, Samsung's devices and the disputed elements of claim 27 of the `338 patent are discussed below. For the purposes of this infringement analysis, all of Samsung's products are addressed together.[87] See FF V 119, 136.

1. **Erase Electrode Element**

[[C]]in Samsung's flash memory devices constitutes an erase electrode as that term is used in claim 27 of the `338 patent. See FF V 123. As noted above, "erase electrode" is properly defined in the context of claim 27 as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. See, supra, at 51. [

[C]

] FF V 125-131. This functionality squarely falls within the properly interpreted scope of the term "erase electrode."

Samsung attempts to avoid a finding of infringement by reading

[87] The Samsung devices are not addressed as having "old" or "new" designs for the purposes of an infringement analysis under claim 27 of the `338 patent. Samsung's redesign was directed at the multi-block erase feature of its devices, which is not the subject matter of the `338 patent.

additional limitations into this element (e.g., that there must be a separate erase electrode for each cell, or that it must be "physically distinct" from any other structure in the device). However, there is no language in the patent or the file history that would require the imposition of these limitations or otherwise vary the ordinary meaning of the term. Thus, the erase electrode limitation must be properly interpreted (as both SanDisk and OUII have argued) in accordance with its ordinary meaning and without Samsung's additional proposed limitations. Applying this interpretation, Samsung's flash memory devices clearly satisfy the "erase electrode" element.

The Administrative Law Judge finds that given its proper interpretation, the term "erase electrode" is broad enough to encompass Samsung's devices under the standards of literal infringement. However, SanDisk and Samsung have raised the issue of the doctrine of equivalents with respect to this claim element.

As an alternative to literal infringement, Samsung's devices would satisfy this claim limitation under the doctrine of equivalents. Samsung argues that its devices do not satisfy this element under the doctrine of equivalents because there are differences between [[C]] and the erase gate disclosed in the preferred embodiment. See, e.g., Respondents' Post-Hearing Br. at 22.

The relevant inquiry under the doctrine of equivalents is not merely whether there are structural differences between the accused devices and the preferred embodiment, but whether the differences between the claimed erase electrode and the Samsung structure are substantial (e.g., whether one of ordinary skill would have known of the interchangeability of [[C]] and the erase electrode of the preferred embodiment). See Hilton-Davis, 62 F.3d at 1519.

Samsung has not argued that one of ordinary skill would lack knowledge of the interchangeability between [[C]] and a dedicated erase gate. In fact, the record establishes that other companies have used [[C]] instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. See FF III 44; CPFF 265-271; SPFF 102.

Indeed, [[C]] performs the same function (acting as a terminal for receiving erase voltage) in substantially the same way (creating a potential difference between [[C]] and the control gate) which pulls electrons off the floating gate to obtain the same result (removal of electrons form the floating gate) as the erase electrode referenced in claim 27. FF V 126-131.

. Accordingly, if the erase electrode element is not literally satisfied by the [[C]] it is met under the doctrine of equivalents.

2. Increment/Decrement Element

[

[C]

] FF V 134-135. This feature alone satisfies the requirement of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions." See, supra, at 53-57. [

[C]] FF V 136.

Samsung argues that its devices do not satisfy the increment/decrement element of claim 27 because [

[C]

] See Choi, Tr. 1351-1352. Moreover, Samsung's asserted claim construction, requiring that both erase and programming operations be effected by successive applications of voltage, was rejected above.

Accordingly, it is found that Samsung's devices practice this element of claim 27.

3. **Temporary Storage Means**

As discussed above, the element "means for temporarily storing a chunk of data for programming a plurality of addressed cells" requires data to be stored in a latch or equivalent structure at least until the cell is verified and programming to the cell is inhibited. [

[C]

] FF V 141-144. Accordingly, Samsung's devices fall within the properly interpreted scope of this element.

Samsung's argument that its devices lack this claim element is based on an incorrect interpretation of the relevant claim language. In particular, Samsung contends that this element must be construed to require data to be stored "during the entire programming process." Respondents' Post-Hearing Br. at 22. That proposed construction of the claim was rejected above.

Samsung also argues that its devices [[C]

] Respondents' Post-Hearing Br. at 23.

However, this argument is contradicted by Samsung's own technical documentation. [

[C]

] Id.

Although the terminology is somewhat different, the function carried out in Samsung's devices is the exact same function performed by the temporarily stored data in the '338 patent. See FF V 144; CX 2 ('338 Patent) at col. 19, line 42 through col. 20, line 16. Accordingly, Samsung's devices satisfy this means-plus-function element."

4. Parallel Programming Means

Both SanDisk's infringement expert and Samsung's infringement expert agree that Samsung's flash memory devices perform the function of programming

---

" [

[C]

] Respondents' Post-Hearing Br. at 23. As set forth above, these alleged differences do not place the Samsung devices outside the scope of this claim element. Aside from these "differences," [

[C]

], and satisfy the second prong of a "means-plus-function" analysis. FF V 142-144.

in parallel into the addressed cells." FF V 145-146.

Nevertheless, Samsung contends that its devices do not satisfy this element because they do not perform the programming function in the same manner as the Hot Electron Injection programming method described in the preferred embodiment of the `338 patent. However, as explained above, claim 27 contains no limitation as to the manner or method of programming. Indeed, from the perspective of the patented invention, there is no difference between programming using Fowler-Nordheim tunneling and programming using Hot Electron Injection inasmuch as both force electrons through the oxide onto the floating gate, which is all that is needed to program a flash memory.

Accordingly, it is found that Samsung's devices practice this claim element.

5. **Verifying Means**

Samsung's flash memory devices perform the function of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data." See FF V 152. [

[C]

" Samsung's devices do not have a source mux or drain mux as shown in Figure 14 of the `338 patent. FF V 148. However, because Samsung uses a NAND architecture, the functions of the muxes can be performed without using these structures. It is logical not to use such muxes in the Samsung designs. FF V 149-151. The logical elimination of these unnecessary structures does not affect the infringement analysis with respect to this means-plus-function claim element. See Data Line Corp. v. Micro Technologies, Inc., 813 F.2d 1196, 1202 (Fed. Cir. 1987) ("We conclude that a reasonable jury could have found that a single sensor with multiplex switching is the equivalent of multiple sensors with multiple switches, and that these are within the scope of the limitation `means for sensing' in claim 1.").

] FF V 154.

The arguments by Samsung and OUII that Samsung's devices lack the claimed verifying means are based on a flawed interpretation of the relevant claim language. It is argued that the Samsung devices do not perform the function of "verifying the programmed data ... with the chunk of stored data" because [[C]

] See SPFF 305; RPFF 458. However, the `338 patent does not require verification of cells that are targeted to be in the erased state. Indeed, as detailed above, the `338 patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at least K - 1, or preferably K reference levels need be provided." CX 2 at col. 11, lines 56-58. In other words, in the case of a two state device, only a single reference level need be used for performing the verification function (i.e., where "0" equals the programmed state, the device only needs to determine whether the cell has reached the "0" state, and can ignore cells targeted to remain in the erased state). The `344 patent (which is incorporated by reference into the `338 patent) similarly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (or erased) and "0" (or programmed).

As discussed above, before a flash EEprom sector can be programmed, it must be erased. See FF V 158. As a result, all of the cells in the sector are necessarily in the erased state at the beginning of the programming process. In a binary implementation of the `338 patent, cells targeted to be in the erased state are then automatically inhibited from programming before

the first pulse is applied. FF III 68.[90] Thus, it would be obvious to anyone of ordinary skill in the art that there is no reason to verify repeatedly whether cells targeted to be in the erased state are in fact in the erased state, since absent a device failure, there is no way for such cells to come out of the erased state that they were in at the beginning of the programming cycle.[91] FF III 71; Pathak, Tr. 823-831; Mehrotra, Tr. 342-351.

Accordingly, the evidence shows that Samsung's devices perform the "verify" function recited in the `338 patent.[92]

Both Samsung and OUII argue that Samsung's devices do not satisfy the "means for verifying" element either literally or under the doctrine of

---

[90] Samsung has proposed a finding that: "Cells in the `338 patent that are to remain in the erase state never encounter programming conditions, and, therefore, there is no need to make a change in their programming conditions." See RPFF 479 (citing Harari, Tr. at 266).

[91] Indeed, at the hearing, Samsung's expert Dr. Allen testified that the M293, a device alleged to invalidate the `338 patent, "does meet the language of the claim in `338," even though that device performed a verify operation "just in the case of going from zero to one." (i.e., only for cells targeted to be in the programmed state). Allen, Tr. 1179-1180; see also Gross, Tr. 1447-1452; CX 204 (concerning the fact that M293 only verifies cells targeted to be in the programmed state, and performs no verification on cells targeted to remain in the erased state). The same type of verification is performed by the Samsung devices. FF V 152-157.

[92] Samsung also argues that it does not verify the programmed data with the chunk of stored data because it does not store "program data," and there is "no temporary storage of data for programming." Respondents' Post-Hearing Br. at 25. As set forth previously in connection with the temporary storage means, the differences between the Samsung devices and the `338 patent with respect to the storage of "program data" are largely semantic, while in other instances Samsung has in fact referred to the stored information as "program data." See CX 56. [

[C]

] See FF V 135, 153-154. This is precisely what is claimed in the `338 patent.

equivalents, because their circuitry is not equivalent to that described in the `338 patent.

As noted above, the `338 patent specifically contemplates a binary device in which a single reference level is used. See SPFF 133-134; CPFF 775. A person of ordinary skill seeking to implement Figure 11-E in a binary device with a single reference level (as is disclosed in the `344 patent at col. 11, lines 56-58) would only use a single sense amplifier to perform that function. See FF III 71-72. Moreover, in its discussion of Figure 11-E, the `344 patent specifically acknowledges that for a four-state device, "only three sense amplifiers and three reference levels are required to sense the correct one of four states," and that a single sense amp and a single reference level can be used to "differentiate correctly between conduction states '1' and '0'." FF V 163; CX 3 (`344 Patent) at col. 26, lines 51-60. Thus, the `344 patent explicitly teaches that for a binary device, only one sense amplifier and one reference level is required to sense the correct state. Finally, the `344 patent specifically discusses an embodiment of Figure 11-E in which "a single sense amplifier" is used. FF V 164; CX 3 at col. 26, lines 8-15. These disclosures are more than adequate to support the conclusion that Figure 11-E would be reduced to a single sense amplifier in a binary device, and that such a structure is the structural equivalent of Figure 11-E.[93]

[

[C]

---

[93] The testimony of Samsung's expert, Dr. Allen, also supports this interpretation. Dr. Allen testified that one of ordinary skill in the art would use a single sense amplifier to verify the programming of a binary device. Dr. Allen further testified that the M293, which uses a single sense amplifier (and no comparator circuit) to perform the verify operation, satisfies the "means for verifying" element of claim 27. Allen, Tr. 1173-1180; see also FF III 71, IV 136.

[C]

] FF V 154. As set forth above, this structure is identical to, or at the very least the structural equivalent of, the structures disclosed in the '338 patent for binary simplifications of Figure 11-E. FF V 155-157. Accordingly, Samsung's devices satisfy this element as properly construed.

6. Inhibiting Means

Samsung uses [[C]]to perform the function of "inhibiting further programming of correctly verified cells among the plurality of addressed cells." The latch used by Samsung is equivalent to latch 721 in Figure 16 of the '338 patent. See FF V 166-171.

Samsung argues that it does not practice this element because it performs the claimed function in a different manner than the preferred embodiment in the patent. This claim element is written in means-plus-function form. The law provides that if an accused device employs a structure that is identical or equivalent to that disclosed in the specification in order to perform the identical function required in the claim, then infringement will be found. Valmont, 983 F.2d at 1042.[24] Claim 27 contains no limitation concerning the manner in which a covered structure is to operate, and Samsung has provided no legal basis upon which to find that infringement may be avoided because of the manner in which the structure operates.

Indeed, Samsung's devices perform the function of inhibiting further

[24] See also Intel Corp., 946 F.2d at 842; D.M.I., Inc. v. Deere & Co., 755 F.2d 1570, 1575 (Fed. Cir. 1985).

programming of a correctly verified cell, until all cells in the chunk have been verified. Pathak, Tr. 840-846; SPFF 312. As in the '338 patent, the inhibiting function is accomplished in Samsung's products [

[C]

] SPFF 313.

[

[C]

] Thomas, Tr. 1119-1120; SPFF 315. In contrast, flipping the latch 721 disclosed in the '338 patent causes 0 volts to be applied to the drain of the disclosed NOR cell. FF V 177; SPFF 316 Nevertheless, no additional structure is required with respect to the latch 721 in order to accomplish the inhibiting function claimed in the '338 patent. Samsung's products therefore include the inhibiting means recited in claim 27.

7. Final Means-Plus-Function Element

In denying that it practices the final element of claim 27, Samsung's only argument is that this final element incorporates three previous elements (parallel programming means, means for verifying, and means for inhibiting further programming) that Samsung contends are not present in its devices. Respondents' Post-Hearing Br. at 27-28. Inasmuch as Samsung practices those three claim elements, Samsung also practices this final claim element. See FF V 179-183.

Conclusion

Based on the foregoing analysis of Samsung's devices, the Administrative Law Judge finds that Samsung infringes claim 27 of the '338 patent literally, or in the alternative, under the doctrine of equivalents.

B. Construction of Claim 27 of the `338 Patent

39. Claim 27 of the `338 patent is as follows:

> In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:
>
> means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

CX 2/RX 5 (`338 Patent) at col. 26, lines. 28-54.

40. The term erase electrode" is found in the `338 patent only in the claims. CX 2; see CFF 257; SFF 98.

41. The term "electrode" is commonly understood in the semiconductor industry as a terminal to which an electrical signal is applied to perform some function. Pathak, Tr. 792, 918.

42. An "erase electrode" is understood in the semiconductor industry as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. Pathak, Tr. 792.

43. Various structures or terminals in a flash memory device can function

also as an erase electrode as that term would be commonly understood, including the silicon substrate. Harari, Tr. 77-83.

44. Various companies have used the substrate instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. Harari, Tr. 77-83; CPX 25.

45. The word "or" in this instance serves its normal function of indicating the availability of an alternative or a choice. See Webster's at 1585.

46. The increment/decrement element of the preamble of claim 27 corresponds to the programming algorithm illustrated in Fig. 15 (item 6), which is described in the text at col. 19, line 57 through col. 20, line 16), whereas the erasing algorithm is illustrated separately in Fig. 11 (items 1 and 2), which is described at col. 16, lines 18-25.

47. The preferred embodiment disclosed in the specification provides examples of incremental programming and of incremental or decremental erasing. See CX 2 at col. 18, lines 21-29.

48. The application of voltage conditions for programing and the application of voltage conditions for erasing are independent of each other. Harari, Tr. 1861, 1870.

49. In both binary and multistate devices, one may design for incremental programming and/or for incremental erasing. However, programming and erasing are not part of the same operation. Harari, Tr. 1869; Pathak, Tr. 937.

50. The consequences of over-erasing are endurance-related. The effect of over-erasing, even in a multistate device, is not catastrophic to the performance of the device. Harari, Tr. 1870; Guterman, Tr. 577-578.

51. With respect to the '338 patent, after the programming of a cell is completed, the information used to program that cell is not used again. Harari, Tr. 248-249.

52. The term "temporarily" ordinarily means "for a brief period: during a limited time: briefly." Webster's at 2353.

53. The "temporarily storing" means of claim 27 is disclosed in Figure 5, including block 190 (labeled "Read/Program Latches and Shift Registers"). Harari, Tr. 247-249; Thomas, Tr. 1509-1511; CX 2, at col. 19, line 27 through col. 20, line 36.

54. The data may be stored in the latches until verification has occurred for the entire chunk of data stored therein, although there is no express requirement to that effect. Thomas, Tr. 1510-1511; Pathak, Tr. 939.

55. After a particular cell to be programmed is verified, the data stored in the latch 190 serves no function for the cell that is already programmed, while the programming continues for the rest of the chunk. Harari, Tr. 247-249; Mehrotra, Tr. 329; Guterman, Tr. 587-588.

56. One of ordinary skill in the art knows that once programming and verification has taken place, the job is done, and "temporarily" in that case would mean just until the job is done. Pathak, Tr. 940-944.

57. Figure 14 of the '338 patent discloses certain structures with which the parallel programming function required by the preamble of claim 27 can be performed. CX 2 at col. 5, lines 40-41; col. 19, lines 27-41; Mehrotra, Tr. 330.

58. In particular, Figure 14 shows an embodiment in which a Program Circuit with Inhibit, block 210, performs the parallel programming function, with the source multiplexer (or "mux") 107 and the drain mux

109 providing the data path. CX 2 at col. 19, lines 27-41; Mehrotra, Tr. 330-334.

59. The cells in the preferred embodiment of the `338 patent are connected in a NOR architecture configuration. Pathak, Tr. 812-813.

60. HEI programming is thus appropriate for use with the cells described in the preferred embodiment. Harari (Tutorial), Tr. 51-52; Mehrotra, Tr. 334-335.

61. The language of claim 27 is silent on the cell structure and the corresponding programming method that must be used. It merely recites the broad, general function of "programming in parallel" without specifying how that programming occurs. One of ordinary skill in the art would know that parallel programming can be achieved through more than one method depending on the type of cell structure selected in a device. Furthermore, circuit designers are familiar with the various methods of programming cells depending upon their structures. Pathak, Tr. 944-946; Harari, Tr. 1861-1865.

62. In claim 27 of the `338 patent, "programming in parallel" means that programming takes place for more than one cell at a time, such that all cells selected for programming by a chunk of data receive programming conditions at the same time. See Harari, Tr. 76; Pathak, Tr. 807-808; CX 2 at col 19, lines 30-31 ("The EEprom array 60 is addressed by N cells at a time.").

63. The term "verifying" as it is used in claim 27 of the '338 patent normally would be understood by one of ordinary skill to refer to the process of determining whether the data in a memory cell matches the data that is targeted to be written into the cell. Guterman, Tr. 489-490, 499. There is no contrary definition of the term in the `338

patent. CX 2.

64. Mr. Thomas, Respondents' expert on whether Complainant SanDisk practices the '338 patent and on whether Samsung infringes the '338 patent, testified that the term "verify" is ordinarily used very loosely in the semiconductor industry to refer to the process of determining whether a cell is finished programming. Thomas, Tr. 1594-1595.

65. In a multi-state device, such as that described in the `338 patent's specification, a cell can be in one of several states. In performing the verification function, the first step is to determine the state of the cell to be verified (e.g., 0, 1, 2, 3). After determining the state the cell is in, the next step is to determine whether the cell is in the target state for that cell. If the cell is in the target state, the cell is verified; if not, further programming is required. Guterman, Tr. 490-493; CPX 46.

66. In a binary device, before programming can begin all cells must be in the erased state. Guterman, Tr, 493-495; CPX 48.

67. Inasmuch as all cells start in the erased state, if the targeted state of a particular cell is the erased state, then the cell is in the targeted state before the programming cycle begins, and therefore no further action needs to be taken with respect to that cell. Harari, Tr. 264-265; Guterman, Tr. 493-495, 499-503; CPX 48.

68. If the targeted state of a particular cell is the programmed state, and if the cell is not in the targeted state before the programming cycle begins, then programming pulses must be applied to bring the cell to its targeted state. Guterman, Tr. 493-495; CPX 48. For cells targeted to be in the programmed state, the cell is read after each programming pulse to verify whether the cell is in the programmed state

(i.e., reads a "1"). Once the cell is sensed to be in the programmed state, further programming to that cell is terminated. Guterman, Tr. 493-495; CPX 48.

69. Figure 11-E of the '344 patent (which is incorporated by reference into the '338 patent) discloses circuitry that corresponds to the verify means in a multi-state implementation of the claim 27 invention. Figure 11-E depicts a multi-state implementation for a single cell in which the cell is able to hold one of four states. CX 2 at col. 4, lines 23-30; Guterman, Tr. 498-499; CX 3 (the '344 Patent); CPX 64.

70. Figure 11-E of the '344 patent discloses four sense amplifiers, one associated with each of the four states that the cell can hold. Each of the four sense amplifiers senses whether the current passing through the cell is greater or lesser than the reference current corresponding to the state associated with that sense amplifier. In the multi-state embodiment disclosed in Figure 11-E, once the sense amplifiers perform their sensing operation, the results are fed into the comparator disclosed in Figure 11-E, which determines whether the state of the cell matches the targeted state of the cell. Guterman, Tr. 499-503; CX 3, Fig. 11-E.

71. A binary embodiment equivalent to that disclosed in Figure 11-E of the '344 patent would not need all the circuitry disclosed in that Figure for a multi-state implementation. Guterman, Tr. 499-503. In a binary device, it is unnecessary to have more than one sense amplifier to perform the verification function of claim 27, since the only decision or verification that the device has to make is whether the cell is in the programmed state. Guterman, Tr. 499-503; Allen, Tr. 1173; CPX 64, 66.

72. For a binary device, it would be logical for a circuit designer to simplify the structure of Figure 11-E of the '344 patent by eliminating three of the four sense amplifiers and the buffers and circuitry uniquely associated with those sense amplifiers, since they serve no function in a binary device and unnecessarily occupy surface area on the chip. Furthermore, with a single sense amplifier, it is unnecessary to have a separate comparator circuit, since that comparator would merely replicate the function of the sense amplifier. Guterman, Tr. 499-503; CPX 64; CPX 66.

73. Figure 16 of the '338 Patent discloses certain additional structures for performing the verification function in a multi-state device. In the circuit compare module 703 shown in the Figure, the read bits are compared bit by bit with corresponding program data bits, i.e., it is determined whether there is a match between the read and write data. This is performed by XOR (exclusive OR) gates such as 711, 713 and 715 shown in Fig. 16. The specification states that the number of such XOR gates used depends upon the number of binary bits encoded for each cell. The output of the XOR gates passes through a NOR gate 717 whenever all the bits are verified, and node 726 is taken high so that latch 721 is set in the verified state. Once latch 721 is set, the cell inhibited from further programming during subsequent programming pulses that may be applied on the chunk. If, however, the read data does not match the write data, then latch 721 remains in its previous state. Mehrotra, Tr. 339; CX 2 at col. 20, lines 17-51.

74. The '344 patent expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (which could indicate "programmed") and "0" (for "erased").

CX 3 at col. 26, lines 55-60. The `344 patent teaches that in a four-state storage device the comparison may be accomplished with four consecutive read cycles and only one sense amplifier, with a different reference applied at each cycle, if the additional time required for reading is not a concern. CX 3 at col. 25, line 64 through col. 26, line 17.

75. The Figure 16 multi-state embodiment could be modified for a binary device by making some simplifications to the structures that would be obvious to an ordinary flash memory circuit designer. Mehrotra, Tr. 342; Pathak, Tr. 819-820.

76. The `338 patent contemplates an embodiment with only two states. The '338 Patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at least K - 1, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed ...." CX 2 at col. 11, lines 56-61.

77. It would be obvious to a circuit designer of ordinary skill to eliminate all but one of the XOR gates (711, 713, 715) in a binary device, since only one bit is being stored in the cell (i.e., "L" = 1). Mehrotra, 342-343; CPX 120; Pathak, Tr. 820-822; CPX 122.

78. In a binary device, it would be obvious to a circuit designer of ordinary skill to change NOR gate 717 of the `338 patent to a single inverter, since there would only be a single XOR gate, and therefore only a single input. Mehrotra, Tr. 342-345; CPX 120; Pathak, Tr. 820-822; CPX 122.

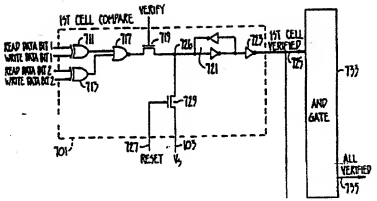
79. In implementing Figure 16 of the `338 patent in a binary device, the

possible combinations of read (R) and write (W) are greatly reduced, as compared to a multi-state device, such that it is not necessary to implement the logic inherent XOR (exclusive OR) gates and NOR gates to verify a cell. Thus, one would expect to make additional simplifications to the circuitry shown in Figure 16 by eliminating entirely the XOR gates and the NOR gate 717. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128.

80. In a binary device, there are only four logically possible states: R=0 and W=0; R=0 and W=1; R=1 and W=0; R=1 and W=1. For example, in the first scenario (R=0 and W=0), the data read from the memory is zero (erased) and the data desired to be written into the memory is also zero. Note also that the third scenario (R=1 and W=0) should not be possible because all cells are required to be in an erased state before programming starts. Mehrotra, Tr. 345-346.

81. Figure 16 of the '338 patent discloses one embodiment of the compare circuit used in the multi-state, preferred embodiment. Figure 16 also discloses circuitry that inhibits further programming of the memory cells. CX 2 at col. 20, line 17-18; Mehrotra, Tr. 340.

82. The pertinent circuitry is depicted in Figure 16 of the `338 as follows:



This illustration, like the illustration contained in Respondents' reply brief, depicts the circuitry of one compare module contained in the preferred embodiment (compare module 701). Figure 16 and the text of the specification provide for "N compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col. 20, lines 18-20, Fig. 16.

83. In the circuit shown in Figure 16, a latch 721 performs the function of inhibiting further programming to correctly verified cells. Mehrotra, Tr. 340-342.

84. When a cell is correctly verified, the result is sent to latch 721, which is then set to the verified state. Mehrotra, Tr. 340; CX 2 at col. 20, lines 28-32.

85. The specification mentions that at the end of a programming pulse all the latches are reset to the unverified state. Node 726 can only be reset by transistor 729 and not by node 717 after node 726 goes high. Mehrotra, Tr. 371-372. Once latch 721 is set in the verified state, the cell is inhibited from further programming during any subsequent

programming pulses which may be applied. Latch 721 in Figure 16 is a "one-way latch." Mehrotra, Tr. 340.

86. The `338 patent specification teaches that "[p]rogramming and verification are repeated until all the cells are correctly verified." FIG. 15(7). Thus, each cell must be read to determine whether the read and write data for that cell match. The specification does not teach that the verification process is to occur repeatedly, i.e., after a cell has been verified. CX 2 at col. 20, lines 14-16.

87. Latches are often referred to as "one-way" or "two way." One-way latches and two-way latches are often drawn in the same manner. Mehrotra, Tr. 372, 397. Yet, they function differently. A two-way latch freely switches back and forth between two states when different input values are applied. Thus, if the input to the latch is a 0, then the value saved in the latch becomes a 0. If a subsequent input is a 1, the latch then saves a 1. However, a one-way latch is said to move in only one direction. Allen, Tr. 1077.

88. With a one-way latch, when verification occurs and the latch is set to a "1", the latch does not go back to a zero during the overall cycle of iterations. Allen Tr. 1078.

89. A one-way latch like that used in Figure 16 of the `338 patent will not allow the detection of so-called "program disturb conditions" where, due to defects in a part, a cell goes back to an erased state before the entire chunk of data is verified. Nor will a one-way latch allow the detection of conditions in which a part fails and a cell is disturbed from an erased into a programmed state. Harari, Tr. 250-252; Mehrotra Tr. 374-378; CX 2.

90. Neither claim 27 of the `338 patent, nor the specification mentions

the detection of program disturb conditions. CX 2.

91. With respect to Figure 16, the specification teaches that the output of the XOR gates passes through NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the bits are verified, otherwise a "0" appears there. When verification occurs (i.e. "[w]hen the control signal VERIFY is true"), "this result is latched to latch 721 such that the same result at the output of NOR gate 717 is also available at the cell compare module's output 725." CX 2 at col. 20, lines 25-32 (emphasis added). The output 725 is fed through an output line to the "program circuit with inhibit 210 of FIG. 5." CX 2 at col. 20, lines 33-36.

92. The specification in describing the functions of latch 721 states that "[w]hen the control signal VERIFY is true, this result is latched to latch 721." It says nothing about resetting latch 721 in case of a subsequent (or previous) control signal VERIFY that is not true. Thus, the specification does not provide that it will return to an unverified state during the program and verification of a chunk of data. Indeed, since latch 721 is a one-way latch, once the latch is set, the stored data cannot be affected by the output of NOR gate 717. Mehrotra, Tr. 340-341.

93. The preferred embodiment of the `338 patent is a multi-state device. If latch 721 were not a one-way latch, there would be catastrophic failure of the multi-state device. See McGreivy, Tr. 1697-1708, 1793-1813; CX 2 at col. 19, lines 4-26.

94. The specification provides that in order to change the setting of latch 721:

> At power-up or at the end of program/verify of a chunk

> of data, all cell compare module's outputs such as 725, 727 are reset to the "not verified" state of "0". This is achieved by pulling the node 726 to V_{ss} (0 V) by means of the RESET signal in line 727 to a transistor 729.

CX 2 at col. 20, lines 46-51.

95. If latch 721 were a two-way latch, before the commencement of programming a cell would be read and if found not to be in the correct state, latch 721 would flip back to the not verified state in response to the output of NOR gate 717, and it would not be necessary to reset the latch with the reset signal. Mehrotra, Tr. 399-400.

96. The specification shows that latch 721 can only be reset by the effect of transistor 729. See Mehrotra, Tr. 342. The specification demonstrates that latch 721, once set to the verified state, remains in the verified state during the entire program/verify of a chunk of data. Then, latch 721 is returned to the "not-verified" state by a reset operation in which node 726 is pulled down, as one would expect in the case of a one-way latch. See Mehrotra, Tr. 400; See also, Allen, 1079, 1086.

97. In order to pull down latch 721, one would have to design the circuit shown in Figure 16 to have transistors of the proper size. Mehrotra, Tr. 409; see also Allen Tr. 1079. The '338 patent does not indicate the size of the transistors involved in Figure 16. Nonetheless, one of ordinary skill would know how to size the transistors shown in Figure 16 relative to the size of NOR gate 717 so as to achieve a one-way latch. CX 2; Mehrotra Tr. 404-409.

98. In addition to the disclosure of Figure 16, including latch 721, Figure 5 of the '338 patent contains a block 210 entitled "Program Circuit with Inhibit." This block provides no detail regarding the

specific circuitry that actually inhibits further programming. CX 2; Guterman, Tr. 508-510.

99. Figure 17 shows "one embodiment of the program circuit with inhibit 210 of Fig. 5 in more detail." CX 2 at col. lines 52-53. The one embodiment shown in Figure 17 is relevant to the Hot Electron Injection programming method used in the preferred embodiment. The circuitry in Figure 17 is for removing voltage from the drain of a cell to inhibit further programming. CX 2, col. 20, line 52 through col. 21, line 8; Mehrotra, Tr. 352-353; Guterman, Tr. 511-513.

100. To one skilled in the art, one way of implementing the inhibit means is to combine certain disclosures in Figures 16 and 5, in particular block 190 of Figure 5, which is entitled "Read/Program Latches and Shift Register." The temporary storage latch disclosed in block 190 of Figure 5 can also serve as the inhibit latch 721 of Figure 16 of the '338 Patent. Mehrotra, Tr. 349-351; CPX 120; CX 2, Fig. 16; Pathak, Tr. 835-839; CPX 57C-58C; CPX 124-125.

101. A flash memory designer of ordinary skill would seek to combine the functions of the temporary storage latch and the verify inhibit latch in a single structure in order to save transistors, thereby reducing the surface area of the chip. Pathak, Tr. 839-840.

102. Figure 16 of the '338 patent discloses structures that correspond to the final means-plus-function element of claim 27 in a multi-state implementation. Those structures include the one-way latch 721, the outputs such as output 725, as well as AND gate 733 whose single output 735 is used to signal the controller in the preferred embodiment that all cells in the chunk of data have been correctly verified. Mehrotra, Tr. 341; CX 2 at col. 20, lines 18-51.

103. The specification provides in part: "[a]s soon as the programmed state is verified correctly, programming stops." CX 2 at col 18, lines 24-25.

104. The patent provides that "parallel programming is implemented in the preferred embodiment of the '338 Patent by a selective programming circuit which disables programming of those cells in the chunk that have already been verified correctly." CX 2 at col. 19, lines 13-16.

105. The patent also provides that "it is preferable to apply programming voltages in repetitive short pulse with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates." CX 2 at col. 9, lines 13-18.

106. Each of the specification passages cited above clearly indicate that the '338 patent will not apply an additional programming pulse to a cell after it has been verified. See Mehrotra, Tr. 253-254; McGreivy, Tr. 1693-1696.

107. Dr. McGreivy explained that failure to terminate will, over time, overstress a binary device and make a multi-state device malfunction. McGreivy, Tr. 1697-1708, 1793-1813. This point is addressed in the text of the '338 patent, as follows:

> In the prior art EEprom devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller 140 or the CPU 160 for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.
>
> In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This

feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue pass [sic] [past] the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEprom chip and the controller, and program verification speed is greatly enhanced.

CX 2 at col. 19, lines 4-26.

know, depending on the type of technology and cell he was working with, whether to apply a resistor, charge pump or some other circuit to apply the erase voltage to the selected sectors. Mehrotra, Tr. 387-388; McGreivy, Tr. 1651-1652.

93. According to Dr. Allen, a person of ordinary skill in the art that pertains to the Mitsuishi `997 patent has the same level of skill as that which pertains to the `752 patent, and provides enough information to enable a person of ordinary skill in the art to construct a EEprom system as disclosed in the `752 patent; yet, the Mitsuishi Patent does not disclose any circuit mechanism for generating an erase voltage. Allen, Tr. 1135-1136.

94. [RESERVED]

95. [RESERVED]

96. Samsung's expert, Dr. Allen, admitted that the `752 patent is a logic level disclosure. Allen, Tr. 1003-1004, 1122.

97. Dr. Allen admitted that one of ordinary skill in the art of the `752 patent would know to use AND circuitry to connect the two signals coming into the sector selected for erase. Allen, Tr. 1123-1125, 1128-1129.

B. The `338 Patent

Anticipation

The M293

98. Samsung introduced an M293B1 television tuner device manufactured by SGS Thomson ("the M293") as a potentially relevant item of prior art. RX 309.

99. The M293 does not perform the function of permanently "inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly" as required by the last element

of claim 27. McGreivy, Tr. 1691-1693, 1793-1794; RT 1818, 1830-1831, 1843; RX 180 at 12-13 and Exh. 1, Sheet 7; CPX 73; CX 199; RX 71.

100. The M293 permits the application of additional programming pulses to an already verified cell. McGreivy, Tr. 1691-1693, 1793-1794; Mehrotra, Tr. 1818, 1830-1831, 1843; Gross, Tr. 1453-1454; RX 180. at 12-13 and Exh. 1, Sheet 7; CPX 73; CX 199; RX 71.

101. The M293 "conditionally" or "temporarily" inhibits the programming of verified cells on a pulse-by-pulse basis. Gross, Tr. 1453-1454; RX 180 at 12-13 and Exh. 1, Sheet 7; McGreivy, Tr. 1691-1693, 1793-1794; Mehrotra, Tr. 1818, 1830-1831, 1843; CPX 73; CX 199; RX 71; CPX 73; CX 199.

102. The M293 does not possess any structure that is capable of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1115; RPX 43; RX 180, at 12-13, Exh. 1, Sheet 7; McGreivy, Tr. 1687-1690, 1691, 1787-1788; CX 199.

103. The M293 device does not possess the one-way latch that is disclosed in circuit 721 of Figure 16 of the `338 patent. Allen, Tr. 1115; RPX 43, RX 180, at 12-13, Exh. 1, Sheet 7; CX 2, at Fig. 16.

104. The "temporary" or "conditional" inhibit present in the M293 would not function for a multistate device. McGreivy, Tr. 1699-1701.

105. The permanent inhibition of verified cells disclosed in the `338 patent is critical to the successful operation of multistate devices. McGreivy, Tr. 1699-1701, 1706.

106. The element in claim 27 which requires permanently inhibiting the programming of verified cells is beneficial to binary NAND devices. Harari, Tr. 73, 1863-1865, 1867-1868; Choi, Tr. 1409.

107. CX 204 is a true and correct copy of a report entitled "An Analysis of

SGS Thomson M293B1 EPM32: Electronic Program Memory for 32 Stations" that was prepared by Chipworks, Inc. ("Chipworks Report"). CX 204.

108. The Chipworks Report is an analysis of the SGS Thomson M293 device that was jointly commissioned by SanDisk and Samsung. CX 204, cover page.

109. The Chipworks Report was the result of extensive reverse engineering analysis of relevant internal circuits of the M293. CX 204 at 1.

110. The Chipworks reverse engineering analysis included a review of the following documentation: (1) the TAEUS Technology Analysis Report entitled "SGS M293 Electronic Program Memory Device ("TAEUS Report") (RX 180C); (2) M293 Data Sheet (RX 98); (3) SGS Technical Note 153 (RX 96); and (4) an article by Guido Torelli entitled "An Improved Method For Programming A Word-Erasable EEPROM" ("Torelli Article"). CX 204 at Tabs 5-8.

111. The Chipworks reverse engineering analysis included removal of the plastic package surrounding the chip and photographing of the relevant circuits. CX 204 at 12, Tab 2.

112. The Chipworks analysis included the microprobing of the internal bit lines of the M293 in order to observe the voltage waveforms during programming and read cycles. CX 204 at 12.

113. In order to microprobe, it was necessary for Chipworks to (1) jet etch a hole through the plastic package to expose the die and (2) remove the scratch protection layer by a wet acid etch to allow direct contact to the metal interconnect lines. CX 204 at 12.

114. The test jig used by Chipworks to test the M293 was constructed around a 28-pin ZIF socket to hold the M293 during the test. CX 204 at 12.

115. In the morning test session of October 15, 1996, the probe tip used to

contact a bit line was connected to a Tektronix TDS380 digital real time oscilloscope via a 10x attenuating probe having an impedance of 14.1 pF and 10 Megaohms. CX 204.

116. In the afternoon test session of October 15, 1996, the oscilloscope was changed to a Tek TDS700A series unit with a 10x attenuating probe of higher impedance: 8.0pF and 10 Megaohms. CX 204.

117. A single M293 device was used for all measurements. CX 204 at 13.

118. Only one bit line was probed for any given measurement depicted in the waveforms attached to Tab 4 of the Chipworks Report. CX 204 at 13, Tab 4.

119. Electrical tests and measurements were made on 6 arbitrary bit lines. CX 204 at 13.

120. All electrical measurements were made at room temperature. CX 204 at 13.

121. The electrical test measurements were made in a semi-darkened room to reduce the light striking the die to a very low level. CX 204 at 13.

122. The test procedures used by Chipworks were agreed to by both SanDisk and Samsung.

123. Both SanDisk and Samsung had representatives present when Chipworks performed the electrical testing.

124. The Chipworks Report confirms the testimony of Dr. Allen and Dr. McGreivy that the M293 does not possess a structure to permanently inhibit programming. Allen, Tr. 1115; McGreivy, Tr. 1687-1690, 1691, 1787-1788.

125. In the M293, the programming of the selected cell on each column of the array is done by applying a sequence of high voltage programming pulses ("Vpp"). CX 204 at 4.

126. During programming, each individual programming pulse to a cell in the M293 device is followed by a verify read operation. CX 204 at 4.

127. When the M293 is in programming mode, the result of the verify read is retained only until the time of the next potential programming pulse. CX 204 at 4.

128. The verify read of the M293 only controls the application or inhibit of a single programming pulse. CX 204 at 4.

129. Programming in the M293 device stops when only all the cells are verified. The M293 does not possess any structure for permanently inhibiting the programming of correctly verified cells. CX 204 at Fig. A.

130. The M293 does not possess a structure to generate a program "lock-out" signal that will guarantee that no further programming will occur once a verify read operation reads a "1" (i.e., the cell has achieved its target programming state) for the first time. CX 204 at 4.

131. The M293 does not possess any structure to guarantee that no further programming will occur to a cell after a verify read operation reads a "1" for the first time. CX 204 at 4.

132. In the M293, it is possible that after one programming pulse has been inhibited, a subsequent pulse will be allowed on the previously verified and inhibited cell. CX 204 at 4.

133. The M293 stops programming altogether when the verify read operation results in "all one" being read across all bits (cells) of the selected word. CX 204 at 4.

134. The results of the Chipworks Report (the M293 does not permanently inhibit) is fully consistent with the results of (1) the SanDisk test report of the M293 and M296 (CX 199) and (2) TAEUS Report (RX 180C).

Compare CX 204 with CX 199 and RX 180C.

135. The application of an additional programming pulse to an M293 cell that has already been verified is possible if the cell has been programmed into a voltage region which produces a sense amplifier misread. CX 204 at 5-6.

136. The M293 uses a sense amplifier to "read" the state of the cell to determine whether a cell being programmed has achieved the "1" or programmed state. CX 204 at 2, 5-6.

137. Any sense amplifier has a small region of input voltages where the resulting output is uncertain and a misread is possible. CX 204 at 5-6.

138. During programming operations, the M293 applies a programming pulse whenever the cell being programmed reads a "0". CX 204 at 9.

139. In the M293, for those cells that read as a "1" (or the "programmed" state), the programming inhibit circuit prevents programming transistor T1 from being turned on and applying a high voltage to the cell. CX 204 at 2-3, 7, 9.

140. The electrical tests of the M293 conclusively show that the M293 does not possess a lock out that guarantees that additional programming pulses will not be applied to a cell after it has been verified. CX 204 at Tab 4.

141. Each and every waveform generated for the Chipworks Report show that the M293 can apply an additional programming pulse to a cell that has been previously inhibited. CX 204 at Tab 4.

142. The capacitive loading of the testing equipment used by Chipworks could cause a misread of an "almost 1" cell as a "1" subsequent to the programming pulse. CX 204 at 9.

143. The misread of an "almost 1" cell is immaterial to the Chipworks

analysis because it does not affect the conclusion that the M293 does not possess any structure for permanently inhibiting the programming of verified cells. CX 204 at 4

144. For an "almost 1" cell that is incorrectly inhibited from programming, the inhibiting of the programming pulse eliminates the high voltage charge on the loaded bit line to bias the next verify read and allows the cell to be correctly read as a "zero." CX 204 at 9.

145. Using the Chipworks test set-up for the M293, if a cell is inhibited for two or more programming pulses, the application of an additional programming pulse cannot be attributed to the capacitive loading of the test set-up. CX 204 at 9.

146. Using the Chipworks test equipment and set-up for the M293, an electrical test where a cell is inhibited for two consecutive pulses and then has a high voltage applied to it during the application of the third programming pulse necessarily indicates that the cell had been programmed into a region where the sense amplifier read result is uncertain. CX 204 at 10.

147. Tab 4, Trace 10 of the Chipworks Report shows a programming cycle where the M293 inhibited the cell being measured for two consecutive programming pulses before applying an additional programming pulse. CX 204 at 10, Tab 4, Trace 10.

148. Tab 4, Trace 10 of the Chipworks Report shows an electrical waveform that was made under test conditions where the high voltage pulse Vpp was set to 23 volts. A Vpp of 23 volts is 1 volt under the data book specifications. CX 204 at 10, Tab 4, Trace 10; RX 98.

149. Tab 4, Trace 10 of the Chipworks Report shows that after inhibiting two consecutive pulses, the M293 applied an additional programming pulse

to the cell. CX 204 at 10, Tab 4, Trace 10.

150. Tab 4, Trace 12 of the Chipworks Report shows an electrical waveform that was made under test conditions where the high voltage pulse Vpp was set to 24 volts. CX 204 at 10, Tab 4, Trace 12.

151. A high voltage Vpp of 24 volts is within the parameters recommended by the M293 data book. RX 98.

152. Tab 4, Trace 12 of the Chipworks Report shows a programming cycle where the M293 inhibited the cell being measured for two consecutive programming pulses before applying an additional programming pulse. CX 204 at 10, Tab 4, Trace 12.

The Torelli Article

153. Samsung introduced an article authored by Guido Torelli, et. al., entitled "An Improved method for programming a word-erasable EEPROM" (the "Torelli Article"), as a potentially relevant article of prior art. RX 71.

154. The Torelli Article described the operation and characteristics of the M293 device. Allen, Tr. 1044-1046.

155. The Torelli Article does not disclose the function of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1175-1177; McGreivy, Tr. 1687-1690; RX 71 at 490 and Fig. 4; CPX 73.

156. The Torelli Article does not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1175-1177; McGreivy, Tr. 1687-1690; RX at 490 and Fig. 4; CPX 73.

157. The Torelli Article, specifically Figure 4, indicates that the cells being programmed are verified between each and every programming pulse. McGreivy, Tr. 1687-1690; CX 86, at Fig. 4; CPX 73.

158. At most, the Torelli Article, specifically Figure 4, discloses a device that conditionally inhibits the programming of cells on a pulse-by-pulse basis. McGreivy, Tr. 1687-1690; CX 86 at Fig. 4; CPX 73.

159. The Torelli Article does not disclose any structure that is capable of permanently inhibiting the programing of correctly verified cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1689; RX 71 at Fig. 2.

160. The Torelli Article does not disclose any structure, like a one-way latch, that is capable of remembering whether a cell has been previously verified and inhibited during the application of previous programming pulses. Allen, Tr. 1038, 1192; McGreivy, Tr. 1689; RX 71 at Fig. 2.

161. The Torelli Article does not disclose any structure for temporarily storing a chunk of data for programming a plurality of addressed cells. Allen, Tr. 1020, 1191; McGreivy, Tr. 1759; RX 71 at Fig. 2.

162. The Torelli Article does not indicate whether the temporarily stored data is to be stored on or off chip. McGreivy, Tr. 1759, 1762; RX 71 at Fig. 2.

163. The Torelli Article does not disclose any structure for verifying the programmed data in each of the plurality of addressed cells with a chunk of stored data. Allen, Tr. 1034, 1191-1192; RX 71 at Fig. 2.

164. The Torelli Article does not disclose any structure for inhibiting programming of correctly verified cells among the plurality of addressed cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686; RX 71 at Fig. 2.

165. The Torelli Article does not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly. McGreivy, Tr. 1686-1691, 1784; RX 71 at Fig. 2.

166. The failure of the Torelli Article to disclose a structure for (1) "temporarily storing a chunk of data for programming a plurality of addressed cells"; (2) "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data"; (3) "inhibiting further programming of correctly verified cells among the plurality of addressed cells"; and (4) "further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly", would preclude an individual of ordinary skill from building the device disclosed in claim 27 of the `338 patent. McGreivy, Tr. 1685, 1787-1788.

Obviousness

167. An individual of ordinary skill in the art of flash memory design and development has a working knowledge of digital logic. McGreivy, Tr. 1650.

168. A working knowledge of digital logic is obtained by someone working probably about two years in the field of integrated circuit design. McGreivy, Tr. 1651.

169. The skill level of an individual with a working knowledge of digital logic is comparable to a bachelor's level degree and some work experience in the field of integrated circuit design. McGreivy, Tr. 1651. Respondents' expert, Dr. Allen, also testified that the level of ordinary skill in the art pertaining to the `338 patent is a bachelor's degree in electrical or computer engineering, an understanding of digital design, computer architecture, and flash EEPROM cell technology, and a few years of work experience in flash EEPROM technology. See RPFF 56; Allen, Tr. at 1007.

170. Individuals of ordinary skill in the art of flash memory design and development have an understanding of integrated circuit fabrication, so that they understand the design rules and circuitry provided by wafer manufacturers. McGreivy, Tr. 1650-1653.

171. An individual of ordinary skill in the art of flash memory design and development has knowledged of semiconductor testing. McGreivy, Tr. 1650.

172. An individual of ordinary skill in the art of flash memory design and development understands device specifications. McGreivy, Tr. 1650.

173. The level of ordinary skill in the art of flash memory design and development is the same for both the `338 and `752 patent. McGreivy, Tr. 1650-1651.

174. Samsung introduced as potentially relevant items of prior art excerpts from a 1993 SGS Thomson Data Book which pertained to the following devices: the M193A, M193C, M193D, M206, M293, M490 and M491 (the "M193A Data Book," "M193C Data Book," "M206 Data Book," "M293 Data Book," "M490 Data Book," and "M491 Data Book" respectively). RX 91-100.

175. The M293 Databook does not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 98 at SEC39804-05; McGreivy, Tr. 1691, 1687-1690, 1787-1788.

176. The M206 Data Book does not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 100, at SEC39852; McGreivy, Tr. 1691, 11887-1690, 1787-1788.

177. The M490 and M491 Data Books do not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 99, at SEC39820-21; McGreivy, Tr. 1687-1691, 1787-1788.

178. The M293, M206, M490 and M491 Data Books combined do not disclose the

function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1691, 1787-1788; CPX 73.

179. The M293 Data Book does not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 98 at SEC39804-05; McGreivy Tr. 1687-1691, 1787-1788.

180. The M206 Data Book does not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 100 at SEC39852; McGreivy, Tr. 1687-1691, 1787-1788.

181. The M490 and M491 Data Books do not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 99 at SEC39820-21; McGreivy, Tr. 1687-1691, 1787-1788.

182. The M293, M206, M490 and M491 Data Books combined do not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1687-1691, 1787-1788; RX 98, at SEC39804-05; RX 100, at SEC39852; RX 99, at SEC39820-21.

183. Samsung introduced the SGS Technical Note 152 ("Technical Note 152"), authored by Guido Torelli et. al. in 1982, as a potentially relevant item of prior art. RX 95.

184. Technical Note 152 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX 95, at 39736.

185. Samsung introduced the SGS Technical Note 153 ("Technical Note 153"), authored by Guido Torelli et. al. in 1982, as a potentially relevant item of prior art. RX 95.

186. Technical Note 153 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX

96, at SEC39754.

187. Samsung introduced the SGS Technical Note 170 ("Technical Note 170"), authored by Guido Torelli et. al. in 1984, as a potentially relevant item of prior art. RX 95.

188. Technical Note 170 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX 94, at SEC39774-75.

189. Technical Notes 152, 153 and 170 combined do not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

190. There is no suggestion in the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 that these pieces of art should be combined together to build the invention claimed in claim 27 of the `338 patent. McGreivy, Tr. 1787-1788; RX 71, 94-96, 98-100.

191. The record is devoid of any evidence to suggest that an individual of ordinary skill would have attempted to combine the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 to build the invention claimed in claim 27 of the `338 patent. See McGreivy, Tr. 1685, 1787-1788; RX 71, 94-96, 98-100.

192. Dr. Allen, Samsung's validity expert, offered no testimony to suggest that one would know how to combine the Torelli article, SGS data books and SGS technical notes. See Allen, Tr. 1004-1195.

193. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or SGS Technical Notes 152, 153 and 170 do not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1685, 1687-1690, 1787-1788; RX 71 at 490 and Fig. 4; CPX 73; RX 98, at

SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

194. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 do not disclose any structure for inhibiting programming of correctly verified cells among the plurality of addressed cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686, 1784; RX 98 at SEC39804-05; RX 99 at SEC39820-21; RX 100 at SEC39852; RX 95 at 39736; RX 96 at SEC39754; RX 94 at SEC39774-75.

195. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 do not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686, 1784; RX 98, at SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

196. The Torelli Article does not render obvious claim 27 of the `338 patent. See, e.g., McGreivy, Tr. 1685, 1687-1690, 1787-1788; RX 71.

197. The Torelli Article in combination with the SGS data books and technical notes does not render obvious claim 27 of the `338 patent. McGreivy, Tr. 1685, 1687-1690, 1787-1788 RX 71; RX 98 at SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.

198. The function of permanently inhibiting the programming of correctly verified cells would not be obvious to an individual of ordinary skill in the art. Harari, Tr. 1863-1865, 1867-1868.

199. Toshiba, the original designer of the NAND architecture, did not

include a permanent inhibit feature in its original 4Mbit memory product. Harari, Tr. 1863-186.

200. The `338 patent has been and will be crucial to SanDisk's success in the mass storage flash memory market. Harari, Tr. 139-140.

201. Intel Corporation, the world's largest commodity flash memory producer, entered into a licensing agreement for all of SanDisk's patents, including the `752 and `338 patents. CX 115; Harari, Tr. 128-120, 281.

202. Intel Corporation acknowledged that a fair and reasonable royalty for SanDisk patents is [[C]] percent in cash and services, with a cap on payments of $[[C]]per quarter. CX 115 at 8; Harari, Tr. 282-287.

203. In 1994, SanDisk was the worldwide leader in the mass storage flash memory with approximately a 40% market share. Harari, Tr. 138-140.

204. Programming is a very stressful process that reduces the life of an EEprom device. Harari, Tr. 24-25.

205. Dr. McGreivy believed that a misverify could "easily" occur in the M293 device. McGreivy, Tr. 1796.

206. Dr. McGreivy agreed that because precision was not essential for a TV tuner the inability of the M293 to permanently inhibit the programming of correctly verified cells did not prevent the M293 from providing satisfactory performance. McGreivy, Tr. 1802.

207. There is no explicit reference to the M293 device in the Torelli Article. RX 71.

208. There is no structure disclosed in the Torelli Article that would indicate what was meant by the term bit-per-bit intelligent writing. McGreivy, Tr. 1684-1685.

209. Torelli left it to the reader to infer what bit-per-bit intelligent writing meant. McGreivy, Tr. 1684-1685, 1768-1770.

210. The capacitance of the microprobe used to test the M293 device had no impact on the conclusions of the SanDisk test report because the M293 does not have any structure to terminate the programming of correctly verified cells. Mehrotra, Tr. 1835.

211. As Dr. McGreivy testified at the hearing, the deposition response he gave on July 31, 1996 assumed that the individual of ordinary skill in the art had in his or her possession an M293 part to generate a circuit schematics of the part through reverse engineering. Dr. McGreivy's deposition answer was never meant to be applied to a situation where the individual only had the Torelli Article and SGS Public literature in his or her possession. McGreivy, Tr. 1787-1790.

212. The SGS data book and technical notes disclose only the recommended voltage conditions. RX 94, RX 95, RX 96, RX 97, RX 98, RX 99.

213. The capacitance of the microprobe used to test the M293 device had no impact on the conclusions of the SanDisk test report because the M293 does not have any structure to terminate the programming of correctly verified cells. Mehrotra, Tr. 1835.

214. Claim 27 of the `338 patent does not make any reference to the use of reference cells during a programming operation on the plurality of addressed cells. CX 2 at 26.

215. In the `338 patent, the verification of a cell is a one-time event. A cell can be "correctly verified" only once during a given programming operation on the chunk of addressed cells. Mehrotra, Tr. 253-254; CX 2 at col. 18, line 1 - col. 19, line 16.

216. The specification of the `338 patent clearly states that disclosed

EEprom device disables the programming of all the cells that have been verified. CX 2 at 19.

217. Dr. McGreivy testified that the following portions of the `338 patent specifications formed in part the basis for his opinion that the last element of claim 27 mandated that the device permanently inhibits the programming of correctly verified cells: column 9, lines 5-17; column 18, lines 17-29; and column 19, lines 10-26. McGreivy, Tr. 1693-1696.

218. As Dr. McGreivy testified, terminating the programming of cells upon verification is an essential feature of multistate device. McGreivy, Tr. 1699-1701, 1706.

219. Dr. McGreivy testified that an EEprom device will experience greater stress and reduced life if programming of cells is not terminated upon verification. McGreivy, Tr. 1699, 1797-1798.

220. Samsung failed to put forth any type of documentary evidence in support of its claim that termination is not an important feature in a multistate device. Allen, Tr. 999-1195.

221. The purpose of the permanent inhibit feature claimed in claim 27 of the `338 patent is to prevent the application of a programming pulse to a cell that has been verified. McGreivy, Tr. 1699-1701, 1706, 1797-1798.

222. In the `338 patent, the verification of a cell is a one-time event. A cell can be "correctly verified" only once during a given programming operation on the chunk of addressed cells. Mehrotra, Tr. 253-254; CX 2 at 18-19.

223. The specification of the `338 patent clearly states that the disclosed EEprom device disables the programming of all the cells that have been verified. CX 2 at 19.

224. Claim 27 of the `338 patent does not make any reference to the use of reference cells during a programming operation on the plurality of addressed cells. CX 2 at 26.

225. As Dr. Harari testified, the permanent inhibit feature of claim 27 would enable a binary device to save power. Harari, Tr. 1864-1865, 1867-1868.

226. Toshiba's NAND products in 1990 and 1991 did not possess a means for terminating programming to correctly verified cells. In 1992, Toshiba's products for the first time contained the termination feature. Harari, Tr. 1867-1868.

The `338 Patent

117. Samsung's flash memory devices are binary devices. CX 56 at 1151 (Samsung IEEE Journal article) ("In program operations, the page buffer latches are first serially loaded with program data: "0" for cells to be programmed and "1" for cells to be inhibited.").

118. Samsung's flash memory devices use a NAND architecture. CX 56 (Samsung IEEE Journal article).

119. Samsung's 4 Mbit, 16 Mbit, 32 Mbit and 64 Mbit flash memory devices operate in substantially the same way with respect to implementation of the `338 patent. Pathak, Tr. 789.

Samsung's Practice of the Preamble of Claim 27

120. Samsung's flash memory devices consist of "an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip" as recited in claim 27 of the `338 patent. Pathak, Tr. 789-790; CX 29 at Bates No. SEC 035132 (Samsung's 1996 data book).

121. Samsung's witnesses did not dispute that Samsung's flash memory devices consist of "an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip" as recited in claim 27 of the `338 patent. Tr. 464-465 (counsel).

122. Samsung's flash memory devices are "of the type having a source, a drain, [and] a control gate" as recited in claim 27 of the `338 patent. Pathak, Tr. 790-791; CX 43, Bates No. SEC 016352 (Samsung product literature).

Samsung's Practice of the "Erase Electrode" Element

123. Samsung's flash memory devices contain "an erase electrode" as that term is used in claim 27 of the `338 patent. Pathak, Tr. 790-791.

124. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

125. [[C]

] Pathak, Tr. 790-794.

126. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

127. [[C]

] Pathak, Tr. 794-794.

128. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

129. [[C]

] Pathak, Tr. 794-794.

130. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56, pp. 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

131. [[C]

] Pathak, Tr. 795.

Samsung's Practice of the Floating Gate Element

132. Samsung's flash memory devices contain "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell," as recited in claim 27 of the `338 patent. Pathak, Tr. 795-796; CX 43 (Samsung product literature).

133. Samsung's witnesses did not dispute that Samsung's flash memory devices contain "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell" as recited in claim 27 of the `338 patent. Thomas, Tr. 1462-1603.

Samsung's Practice of the Increment/Decrement Element

134. Samsung's flash memory devices satisfy the requirement of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions" as recited in claim 27 of the `338 patent. Pathak, Tr. 796-798; CX 52 (Samsung's programming algorithm); CX 56 (Samsung

IEEE Journal article).

135. [[C]

] Pathak, Tr. 796-798; CX 52 (Samsung's programming algorithm); CX 56 (Samsung IEEE Journal article).

136. [[C]

] Choi, Tr. 1351-1352.

137. Neither Mr. Thomas, Samsung's expert on whether SanDisk practices the '338 patent, nor any other Samsung witness offered any testimony to rebut Mr. Pathak's conclusion that Samsung's flash memory devices satisfy the limitation of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions." See Thomas, Tr. 1462-1604.

Samsung's Practice of the Temporary Storage Means

138. Samsung's flash memory devices perform the function of "temporarily storing a chunk of data for programming a plurality of addressed cells." Pathak, Tr. 798-805.

139. [[C]

] CX 56 at 1151 (Samsung IEEE Journal article) [[C]

] Pathak, Tr. 803-804 [[C]

]CPX 59.

140. [[C]
] CX 56 at 1151 (Samsung IEEE Journal article) [[C]
]; CPX 128, line 2.

141. [[C]
] Thomas, Tr. 1584-1585.

142. [[C]
] Pathak, Tr. 799-802; CX 46 (Samsung core schematics); CX 56 at 1150-51 (Samsung IEEE Journal article); CPX 57C; CPX 63C (modification of Samsung core schematic).

143. [[C]
] Pathak, Tr. 802-803; CX 2 ('338 Patent), Fig. 5; CX 56 at 1150 (Samsung IEEE Journal article); CPX 59C.

144. [[C]
] Pathak, Tr. 804-805.

Samsung's Practice of the Parallel Programming Means

145. Samsung's flash memory devices perform the function of "programming in parallel the stored chunk of data into the plurality of addressed cells." Pathak, Tr. 805-808.

146. [[C]] Thomas, Tr. 1590-1591.

147. [[C]] Pathak, Tr. 805-808; CX 46C (Samsung core schematic); CPX 61C.

148. [[C]] Pathak, Tr. 808; Mehrotra, Tr 337.

149. [[C]] Pathak, Tr. 808-812; Mehrotra, Tr. 336.

150. [[C]] Pathak, Tr. 808-813; CPX 137-139.

151. [[C]] Mehrotra, Tr. 336-338; Pathak, Tr. 808-813; CPX 137-139.

Samsung's Practice of the Verification Means

152. Samsung's flash memory devices perform the function of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data." Pathak, Tr. 814-81; CPX 60.

153. [[C]

] Thomas, Tr. 1594-1595; RX 15C at 49 (Expert Report of Mammen Thomas).

154. [[C]

]

Choi, Tr. 1409-1410; CX 56 at 1154 (Samsung IEEE Journal article).

155. [[C]

] Pathak, Tr. 818-819; CX 48C (Samsung 16 MBit NAND functional block diagram); CPX 60C.

156. [[C]

] RX 15C at 49 (Expert Report of Mammen Thomas).

157. [[C]

] Pathak, Tr. 814-820, 829-831, 959-960, 975; RX 205 at 15 (Expert Report of Jagdish Pathak); CX 48C (Samsung 16 MBit functional block diagram); CPX 60C; CPX 127.

158. A flash prom cell must be erased before it can be programmed or reprogrammed. Pathak, Tr. 932-933; CX 2 at col.1, lines 46-54, and col.

19, lines 60-63.

159. [[C]

] Choi, Tr. 1354-1356.

160. The `338 patent discloses that "if each memory cell is to store K states, then at least K-1, or preferably K reference levels need be provided." CX 2 at col. 11, lines 56-58.

161. The `338 patent discloses that in a two-state implementation, only a single reference level is required. CX 2 at col. 11, lines 56-58.

162. The '344 patent, which is incorporated by reference into the `338 patent, discloses that to sense the correct one of K states, only K-1 reference levels and K-1 sense amplifiers are required. CX 3 ('344 Patent) at col. 26, lines 51-55.

163. The '344 patent, which is incorporated by reference into the `338 patent, expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (e.g., or programmed) and "0" (e.g., or erased). CX 3 ('344 Patent) at col. 26, lines 55-60.

164. The '344 patent, which is incorporated by reference into the `338 patent, expressly states that Figure 11-E can be implemented using a single sense amplifier. CX 3 ('39644 Patent) at col. 26, lines 8-15.

165. The '344 patent, which is incorporated by reference into the `338 patent, explicitly discloses that "the same principle employed in the circuit of Figure 11-E can be used also with binary storage." CX 3 ('344 Patent) at col. 26, lines 66-67.

Samsung's Practice of the Inhibit Means

166. Samsung's flash memory devices perform the function of "inhibiting further programming of correctly verified cells among the plurality of

addressed cells." Pathak, Tr. 833-835; CPX 62C.

167. [[C]

] Thomas, Tr. 1597.

168. [[C]

] Pathak, Tr. 833-835; CPX 62C.

169. [[C]

] Pathak, Tr. 833-835, 840-841; CPX 62C, 123, 127.

170. [[C]

] Pathak, Tr. 833-835; CPX 62C.

171. The Samsung flash memory device performs the function of "inhibiting further programming of "correctly verified" cells among the plurality of addressed cells" in an equivalent manner to that disclosed in the '338 patent. Pathak, Tr. 967-969.

172. Dr. McGreivy testified that terminating programming of verified cells will improve the performance of a binary device and prevent it from wearing out a little earlier and is needed in a multi-level device to prevent misprogramming of data. McGreivy, Tr. 1697-1701, 1797-1799.

173. Samsung's devices perform the function of inhibiting further programming of a "correctly verified" cell, until all cells in the chunk have been verified. Pathak, Tr. 842-845; Thomas, Tr. 1597.

174. [[C]

] Pathak, Tr. 840-841

(equating Samsung's page buffer latch with latch 721 disclosed in the patent); CX 56 at 1151, col. 2, lines 21-23); CPX 123 (simplified Samsung verification circuit); CPX 53 (showing Samsung's verification circuit in more detail); CX 56, Fig. 1 (Samsung publication describing the inhibiting scheme); CX 46 C (showing Samsung's most detailed core schematics); Pathak, Tr. 845-846 (equating simplified Samsung circuits to features in core schematics).

175. [[C]

] CPX 60 C

(described at Pathak, Tr. 842-843; CX 56 at 1152, Fig. 5(a); Thomas, Tr. 1519.

176. [[C]

] CX 56 at 1153, col. 1, lines 2-12; Thomas, Tr. 1119-1120.

177. Flipping the latch 721 disclosed in the '338 patent flips causes 0 volts to be applied to the drain of the disclosed NOR cell. Mehrotra, Tr. 332, 352-353; Pathak, Tr. 967.

178. Although the latch 721 in the '338 patent outputs a logical "1" in the non-verified state while [[C]

] (compare CX 2, Col. 20 with CPX 60-C) these differences are insubstantial given that each signal will inhibit programming in its respective NAND or NOR architecture (see Mehrotra, Tr. 338-339) and that

FIG. 16 of the `338 patent includes an inverter 723 which could be removed to provide the logical output required by Samsung (CX 2).

Samsung's Practice of the Final Means of Claim 27

179. Samsung's flash memory devices perform the function of "further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of "correctly verified" cells until all the plurality of addressed cells are verified correctly." Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

180. [[C]

] Pathak, Tr. 844-845.

181. [[C]

] Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

182. [[C]

] Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

183. Neither Samsung's Pre-Hearing Statement nor the hearing testimony of Samsung's infringement expert, Mr. Thomas, disputes that if Samsung's

devices fall within the scope of the verify means and the inhibit means, they also satisfy the final claim 27 means plus function element. Respondents' Post-Hearing Br.; Thomas, Tr. 1462-1604.

DECISION ON APPEAL, *SANDISK CORPORATION V. MEMOREX PRODUCTS, INC.*, 415 F.3D 1278, 75USPQ 2D1475 (FED. CIR. 2005)

granted monopolies like that existing in Tudor England, is not supported by the evidence. As discussed *supra* in note 12, USPTO has issued more than 2 million patents since FY-91, and the requirements that a patentable invention be useful, novel, and non-obvious remain in the statutes, conforming to the constitutional command of the Intellectual Property Clause.

In sum, during the past fourteen fiscal years, USPTO has taken in billions of dollars cumulatively in fees and has provided billions of dollars worth of services, most of which involved issuing more than 2 million patents. USPTO appropriations have increased by a factor of thirteen during that timespan. Congress is, thus, funding USPTO operations, and funding them generously, with money assessed in the form of patent fees, although Congress has not dedicated all of the fees to that particular purpose, choosing instead to spend 4.4 percent of those fees on other priorities. Congress' determination of federal spending priorities and how the patent system fits into national economic development goals is an eminently rational exercise of its power.

Conclusion

Congress is entitled to great deference under the Necessary and Proper Clause when it legislates under its Intellectual Property power. Any intellectual property law Congress passes need only survive the limited scrutiny of the rational basis test as to whether it promotes the progress of science and the useful arts. Plaintiff may well be correct that the current patent fee regime is misguided and creates the wrong incentives, but such policy determinations are for Congress, and not the courts, to make. Plaintiff has not carried his burden of showing that Congress has behaved irrationally.

Having disposed of the case under the Intellectual Property Clause, the court need not reach defendant's Commerce Clause and General Welfare Clause arguments.

Accordingly, plaintiff's motion for summary judgment on his illegal exaction claim is DENIED. Defendant's cross-motion for summary judgment on plaintiff's illegal exaction claim is GRANTED. Plaintiff's motion for class certification, which the court had stayed in an order dated October 7, 2003, is hereby MOOT.

In addition, since the court decides the illegal exaction claim on the merits based on the broad issue of constitutionality, the question of USPTO pension liabilities is MOOT, and plaintiff's alternative motion for additional discovery is, therefore, DENIED.

The Clerk of the Court shall enter judgment for defendant. No costs.

IT IS SO ORDERED.

SanDisk Corp. v. Memorex Products Inc.

U.S. Court of Appeals
Federal Circuit
Nos. 04-1422, -1610
Decided July 8, 2005

PATENTS

[1] Patent construction — Claims — Broad or narrow (§ 125.1303)

Patent construction — Claims — Process (§ 125.1309)

Language of claims directed to "flash" computer memory system that "includes" array of memory cells which are "partitioned into a plurality of sectors" does not require that every electrically erasable programmable read-only memory cell within device be grouped into sector that is partitioned into "user data" and "overhead data" portions, since claimed method requires "partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion," since term "includes" is equivalent to "comprising," and thus does not foreclose additional elements that need not satisfy stated claim limitations, since nothing in recitation of these groupings of flash EEprom cells excludes other configurations of memory cells on physical device that, in some part, practices claimed methods, and since, therefore, nothing in claim language prevents use of flash EEproms containing cells that are not grouped into partitioned sectors.

[2] Patent construction — Specification and drawings — In general (§ 125.1101)

Patent construction — Claims — Process (§ 125.1309)

Specification of patent directed to "flash" computer memory system that includes array

of memory cells which are "partitioned into a plurality of sectors" is incompatible with claim construction that requires every electrically erasable programmable read-only memory cell within device to be grouped into sector that is partitioned into "user data" and "overhead data" portions, since specification describes embodiment in which "sector defect map," containing only "overhead" data, is part of flash EEprom memory, since portions of flash EEprom memory used in such preferred embodiment would not be partitioned into user data and overhead data portions, and since foregoing claim construction would improperly exclude such embodiment; even if it is assumed that invention is directed only to partitioned sectors, language of asserted claims does not preclude other, unclaimed organizations of flash EEprom memory cells, and claim terms are not properly limited to preferred embodiment described in specification.

[3] Practice and procedure in Patent and Trademark Office — Prosecution — Disclaimer (§ 110.0925)

Patent construction — Prosecution history estoppel (§ 125.09)

Patentee, during prosecution of application for patent directed to "flash" computer memory system that includes array of memory cells which are "partitioned into a plurality of sectors," did not clearly and unmistakably disclaim any method or device in which electrically erasable programmable read-only memory cells are not grouped into partitioned sectors, since patentee's description of "each sector" as having both "user data" and "overhead data," considered in context, can be read as referring to "each sector" subject to claimed method, and no more, since arguments explicating claimed invention did not purport to exclude other configurations of flash EEprom memory cells, and since patentee's statement that it sought to have claimed invention emulate disk drive memory configuration does not compel conclusion that patentee required every flash EEprom cell to be grouped into partitioned sectors.

[4] Infringement — Defenses — Estoppel; laches (§ 120.1103)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Defenses — Estoppel (§ 410.1805)

Patent infringement plaintiff is not judicially estopped from arguing broad claim construction asserted in present case, since analysis underlying claim construction in prior litigation did not extend to issue presently at bar, since plaintiff therefore did not advance claim construction in prior litigation that was "clearly inconsistent" with construction asserted in present case, and federal district court in prior case cannot be said to have adopted such position at plaintiff's urging, and since equitable principles do not favor applying judicial estoppel to prevent claim construction arguments from evolving after preliminary injunction stage, as they did in present case.

[5] Procedure — Judicial review — Standard of review — In general (§ 410.4607.01)

Federal district court's application of its local rules are reviewed for determination of whether court's decision was clearly unreasonable, arbitrary or fanciful, or based on erroneous conclusion of law, whether court's findings were clearly erroneous, or whether record contains no evidence upon which court rationally could have based its decision; in present case, district court hearing patent infringement action did not abuse its discretion by refusing to consider defendant's arguments concerning claim construction and infringement that were presented after relevant cut-off dates under court's relevant local rules.

Particular patents — Electrical — EEprom memory system

5,602,987, Harari, Norman, and Mehrotra, flash EEprom system, summary judgment of noninfringement vacated.

Appeal from the U.S. District Court for the Northern District of California, Walker, C.J.

Action by SanDisk Corp. against Memorex Products Inc. (formerly d/b/a Memtec Prod-

ucts Inc.), Pretec Electronics Corp., Power Quotient International Co. Ltd., and Ritek Corp. for patent infringement. Plaintiff appeals from summary judgment of noninfringement. Vacated and remanded.

Donald R. Dunner and Thomas H. Jenkins, of Finnegan, Henderson, Farabow, Garrett & Dunner, Washington, D.C.; Erik R. Puknys, of Finnegan, Henderson, Farabow, Garrett & Dunner, Palo Alto, Calif.; Michael A. Ladra and James C. Yoon, of Wilson Sonsini Goodrich & Rosati, Palo Alto; Michael A. Berta and Ariana M. Chung-Han, of Wilson Sonsini Goodrich & Rosati, San Francisco, Calif., for plaintiff-appellant.

Jon B. Streeter and G. Whitney Leigh, of Keker & Van Nest, San Francisco, for defendant-appellee Memorex Products Inc.

Ronald C. Finley, Daniel S. Mount, Alfredo A. Bismonte, and Justin T. Beck, of Mount & Stoelker, San Jose, Calif., for defendant-appellee Pretec Electronics Corp.

Alan D. Smith and Charles H. Sanders, of Fish & Richardson, Boston, Mass., for defendant-appellee Ritek Corp.

Before Rader, Gajarsa, and Dyk, circuit judges.

Gajarsa, J.

SanDisk appeals the district court's judgment of no infringement in favor of Memorex, Pretec, and Ritek. The district court granted summary judgment that various Flash memory devices made by these defendants did not infringe independent claims 1 or 10—or various claims depending therefrom—in SanDisk's U.S. Patent No. 5,602,987 to Flash EEprom systems. The trial court ruled that the claims at bar did not contemplate or allow for a Flash memory system in which some EEprom memory cells are grouped into sectors that are not partitioned into user and overhead data portions. As the record showed that the defendants' products contained sectors of memory cells lacking such partitions, the trial court determined that these defendants could not infringe. We conclude that the trial court misread the claims at issue, and erred in finding a prosecution disclaimer in support of its reading. We further reject the contention that judicial estoppel forecloses SanDisk's claim construction arguments on appeal. Thus, we vacate the judgment and remand for further proceedings.

I.

A.

SanDisk Corp. ("SanDisk") owns U.S. Patent No. 5,602,987 to Flash EEprom systems ("the '987 patent").[1] The '987 patent issued on February 11, 1997, and describes methods for using EEproms as non-volatile solid state computer memory. A non-volatile memory retains its contents even after power is shut off. This "flash memory" has many applications, including the memory used in digital cameras, PDAs, memory sticks or MP3 players.

Flash EEproms can sustain only a limited number of writes and erases before they fail. The '987 system and methods include innovations directed at improving flash memory performance and extending EEprom life. The patent focuses, in particular, on improving the memory system architecture over the prior art. The memory architecture generally concerns how the memory system solves the problem of storing or retrieving specific information from the memory cells. *See* '987 patent, col. 5, ll. 4-21. If the architecture can be designed to minimize the number of times each EEprom memory cell is erased and rewritten, then that solution can extend the useful life of the integrated circuit. If the architecture allows for faster operations, then the EEprom performance will improve.

The '987 patent addresses these issues in at least two ways relevant to this appeal. First, it introduces a multi-sector erase function. In earlier systems either every memory cell in an EEprom would be written or erased in one operation, or only a single "sector" could be erased in one operation. *See* '987 patent, col. 4, ll. 46-63. Where not all the information was to be erased, systems that operated only on the entire chip had to read that information out, store it in a temporary location (typically a different, volatile memory or RAM), erase the entire chip, and then write the information back into the EEprom memory. *Id.* The other approach, operating sequentially on individual sectors, proved time-consuming.

The '987 patent describes a different way of organizing the memory storage, and in particular arranges memory cells into "sectors" akin to the physical "sectors" used for storage

[1] Electrically erasable programmable read only memory (EEprom).

on magnetic disk drives. The '987 patent allows the operator to select multiple sectors for simultaneous erase. The defining feature of the "sector" of memory cells is that all cells within the sector are erased together. *See* '987 patent, col. 1, ll. 65-66 ("[A]n array of Flash EEprom cells on a chip is organized into sectors such that all cells within each sector are erasable at once."); *id.* at col. 5, ll. 9-11 ("The memory in each Flash EEprom chip is partitioned into sectors where all memory cells within a sector are erasable together."). Put differently, the "sector" is the "basic unit of erase." The '987 patent illustrates this architecture, as implemented on a single EEprom or integrated circuit (chip), in Fig. 3A:

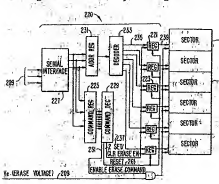
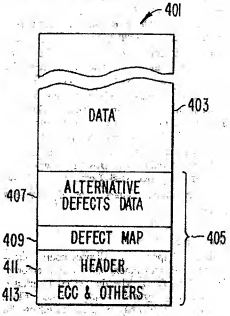


FIG._3A

Although the block diagram in Fig. 3A illustrates the description of multiple sectors on a single chip, the multi-sector erase feature is not limited to individual EEproms. As the '987 patent notes, "the selected sectors [for erase] may be confined to one EEprom chip or be distributed among several chips in a system. The sectors that were selected will all be erased together." '987 patent, col. 5, ll. 16-19. Because this allows more intelligent use of the memory, avoiding needless erases, it improves performance and extends the operational life of the EEproms. As the patent explains, "[t]his is faster and more efficient than prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation." '987 patent, col. 2, ll. 4-7.

Second, the architecture described in the '987 patent further requires "partitioning" the "sectors" into at least two components—one for "user data," and a second for "overhead." "User data" means the information that the processor stores or on which it operates. "Overhead data" refers to administrative information used by the memory controller, such as data address information (typically the information included in a header), memory cell defect maps, error correction code, and so on. The memory allocation in a "typical" sector is illustrated in Fig. 5:



SECTOR PARTITION

FIG._5.

SanDisk argues that this feature "improves the reliability of Flash EEprom memory systems." The written description explains,

> The memory architecture has a typical sector 401 organized into a data portion 403 and a spare (or shadow) portion 405. The data portion 403 is memory space available to the user. The spare portion 405 is further organized into an alternative defects data area 407, a defect map area 409, a header area 411 and an ECC and others area 413. These areas contain information that could be used by the controller to handle the

fects and other overhead information such as headers and ECC.

'987 patent, col. 8, ll. 43-50.

B.

In 1998 SanDisk accused Lexar Media Inc. ("Lexar") of infringing claims 1 and 10 of the '987 patent. The action was assigned to Judge Breyer in the Northern District of California. On March 4, 1999, Judge Breyer issued a claim construction order interpreting the "user data and overhead data portions." He expressly limited the order to "those terms and issue[s] discussed by both parties in their memoranda and at the claim construction hearing." *SanDisk Corp. v. Lexar Media, Inc.*, No. C 98-01115 CRB, 1999 WL 129512, at *2 (N.D. Cal. Mar. 4, 1999).

With that caveat, Judge Breyer ruled that the partitioning and user data / over head data limitations meant that

> Each non-volatile memory sector must have at least one user data portion *and* one overhead data portion, but is not limited to only one data user portion and only one overhead data portion.

Id. at *3. SanDisk eventually obtained a judgment of infringement against Lexar.

C.

In October 2001, SanDisk sued four Flash memory system manufacturers: Memorex Products, Inc. ("Memorex"); Pretec Electronics Corp. ("Pretec"); Ritek Corp. ("Ritek"); and Power Quotient International Co., Ltd., for infringing the '987 patent, claims 1 and 10 (and various dependent claims). In due course Power Quotient was dismissed from suit.

SanDisk sought a preliminary injunction based on Judge Breyer's claim construction. The defendants opposed, and the trial court denied the motion. In assessing the partitioning limitation, the trial court heavily relied on the prosecution history:

> SanDisk specifically limited its claim to include only those devices in which *each* sector within a memory cell array contains both overhead and user data. SanDisk cannot now argue that only some of the sectors of a memory cell array need to contain user data and overhead data.

On September 30, 2003, the district court construed claims 1 and 10 to require that every cell in the memory device be grouped into a sector, and every sector be partitioned into user and overhead data portions. *See SanDisk Corp. v. Memorex Prods., Inc.*, No. C-01-4063 VRW, slip. op. at 34 (N.D. Cal. Apr. 20, 2004) ("Pretec SJ Order") ("[T]he court's claim construction requires all sectors within the memory array to be partitioned.").

Although the trial court's claim construction considered the claim language and the written description, the court relied primarily on a finding of prosecution disclaimer. *Id.* at 28 ("[T]he court finds that SanDisk clearly and unmistakably disclaimed coverage of systems in which only some of the sectors in the array were partitioned into at least user data and overhead portions."); *see also id.* at 16-29.

With that claim construction the trial court granted Ritek summary judgment of non-infringement, because Ritek had presented evidence that their products include some sectors that are not partitioned.

Pretec and Memorex moved for summary judgment on the same ground. The court granted Pretec's motion on April 20, 2004, and Memorex's motion on May 13, 2004, after each party supplemented the record with evidence about their devices.

The trial court entered judgment of no infringement, SanDisk timely appealed, Ritek and Pretec separately oppose, Memorex joins in Pretec's opposition. Pretec adopts Ritek's arguments in opposition by reference, but did not file a separate joinder. The court has jurisdiction under 28 U.S.C. § 1295(a)(1) (2000).

II.

The court reviews *de novo* the trial court's summary judgment of no infringement. *Hilgraeve Corp. v. McAfee Assocs., Inc.*, 224 F.3d 1349, 1352 [55 USPQ2d 1656] (Fed. Cir. 2000). Summary judgment is proper only if the movants are entitled to judgment as a matter of law, and no genuine issue of material fact requires a determination by a fact-finder. *See* Fed. R. Civ. P. 56(c); *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 250 (1986). In this case there are no disputed material facts at issue. The judgment turns solely on claim construction, which the court reviews *de novo*. *See Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 [46 USPQ2d 1169] (Fed. Cir. 1998) (en banc).

A.

The court's claim construction ascribes claim terms the meaning they would be given by persons of ordinary skill in the relevant art at the time of the invention. *See* 35 U.S.C. § 112; *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 [72 USPQ2d 1001] (Fed. Cir. 2004). Claim construction begins with the language of the asserted claims. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 [39 USPQ2d 1573] (Fed. Cir. 1996). The relevant claim language in this case appears identically in independent claims 1 and 10. It provides,

> A method of operating a computer system *including* a processor and *a memory system*, wherein *the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors* that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:
>
> providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,
>
> *partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion* . . . .

'987 patent, col. 16, ll. 24-37 (claim 1, emphases added); *see also id.* at col. 17, ll. 30-44 (claim 10). Although SanDisk also asserted claims 2, 5, 6, 12, and 15 of the '987 patent, each depends from claim 1 or 10 and incorporates the forgoing limitations in relevant part. The parties do not dispute, and the trial court correctly noted, that the preamble recited above is limiting.[2]

Reviewing the partitioning requirement, the trial court concluded that claim 1 and claim 10 require every Flash EEprom memory cell within an actual device to be grouped into a sector that is partitioned into user and overhead data portions. SanDisk argues that this construction misreads the plain language of the claim. The argument proceeds on two levels. First, by its plain language, claims 1 and 10 require only that the claimed memory system contain some memory cells, grouped into sectors, partitioned into user and overhead data portions. Nothing in the claims precludes additional memory cell configurations, which need not contain such partitioned sectors. Second, claims 1 and 10 are self-evidently drawn to claimed methods. It is fully consistent with practicing the claimed invention to make additional, unclaimed use of Flash EEprom memory cells, so long as each limitation is satisfied. We agree.

[1] The invention is claimed using nonrestrictive terminology. The memory system "includes" an array of "non-volatile floating gate memory cells" which are "partitioned into a plurality of sectors." The claimed method requires "partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion." As a patent law term of art, "includes" means "comprising." *See Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1344-45 [65 USPQ2d 1385] (Fed. Cir. 2003); *Hewlett-Packard Co. v. Repeat-O-Type Stencil Mfg. Corp., Inc.*, 123 F.3d 1445, 1451 [43 USPQ2d 1650] (Fed. Cir. 1997). Neither includes, nor comprising, forecloses additional elements that need not satisfy the stated claim limitations. Nor does the choice of articles—"an array" of memory cells, "a plurality of sectors," "said array of memory cells," "the memory cells," or "the individual sectors"—compel a different conclusion. These groupings of Flash EEprom memory cells provide an antecedent basis for various steps of the claimed method, but nothing in their recitation excludes other configurations of memory cells on a physical device that, in some part, practices the claimed methods. Thus, nothing in the language of claims 1 or 10 prevents the use of Flash EEproms containing cells that are not grouped into partitioned sectors.

B.

SanDisk further argues that the '987 patent specification is inconsistent with the trial court's claim construction because, among other reasons, it excludes at least two preferred embodiments: one involving storing a sector defect map in Flash EEprom memory cells, and another involving using Flash EEp

[2] That is, because "when read in the context of the entire claim" the preamble "recites limitations of the claim . . . or . . . is 'necessary to give life, meaning, and vitality' to" claims 1 and 10, the trial court properly treated the language as limiting. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 [51 USPQ2d 1161] (Fed. Cir. 1999).

rom cells as a write memory cache. As explained below, the court need only consider the sector defect map to conclude that SanDisk is correct.

[2] The court must always read the claims in view of the full specification. *See Vitronics*, 90 F.3d at 1582. A claim construction that excludes a preferred embodiment, moreover, "is rarely, if ever, correct." *Vitronics*, 90 F.3d at 1583; *see also C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 865 [73 USPQ2d 1011] (Fed. Cir. 2004). The '987 patent specification describes an embodiment involving a sector defect map, which, in brief, contains information mapping defective memory sectors into good ones. *See* '987 patent, col. 11, ll. 57-60. Although the defect map may be stored in spare, defect-free portions of the affected sector, at some point there will be too many defects to keep the defect map in that location. "Thus, it is preferable in another embodiment to locate the sector map in another memory maintained by the controller. *The memory may be located in the controller hardware or be part of the Flash EEprom memory.*" '987 patent, col. 11, l. 65—col. 12, l. 1 (emphasis added). SanDisk argues that because the sector defect map would contain only overhead data, the portions of the Flash EEprom memory used in the preferred embodiment would not be partitioned into user data and overhead data portions as required by according claims 1 or 10. As the district court's claim construction would foreclose that possibility, the claim construction must be wrong.

The trial court rejected this argument. It ruled, instead,

> The fact that the sector defect map contains only overhead data does not prove that the embodiment contemplates sectors with only overhead data. Although the sector defect map is composed entirely of overhead data, the court finds that the sector defect map is located entirely within the overhead portion of a single sector.

We find this reasoning misplaced.

In its brief to this court Ritek concedes that the sector defect map could be located in "a part of memory outside the array of sectors partitioned into a user data and overhead portions, *i.e.*, in an unsectored part of the memory." Ritek Br. at 43-44. If Ritek is correct, then the trial court's claim construction must be wrong. The claims must allow, instead, for Flash EEprom memory cells that are not sectored, or not partitioned, according to the claimed methods. But since Ritek concedes this point, and both Pretec and Memorex join Ritek's argument, there is no dispute left for the court to resolve. In sum, the trial court's speculative treatment of the preferred embodiment is unsupported by the patent specification, not grounded in the record, and contrary to the reading suggested by all parties. We conclude that SanDisk is correct in faulting the trial court's claim construction.

Ritek contends that the only sectors described in the '987 patent specification are partitioned as illustrated in Fig. 5. Thus, Ritek concludes, the invention is directed only to partitioned sectors. We find this reasoning misplaced for at least two reasons. First, as noted above the language of claims 1 and 10 does not preclude other, unclaimed organizations of Flash EEprom memory cells. Thus, even if the court concluded that Fig. 5 shows the only partitioning consistent with the claimed methods that would not preclude use of other organizations in the memory system. Second, it is axiomatic that without more the court will not limit claim terms to a preferred embodiment described in the specification. *Laitram Corp. v. Cambridge Wire Cloth Co.*, 863 F.2d 855, 865 [9 USPQ2d 1289] (Fed. Cir. 1988) ("References to a preferred embodiment, such as those often present in a specification, are not claim limitations."). The '987 patent specification plainly describes the sector partitioning illustrated at Fig. 5 as a "typical" sector organization. *See* '987 patent, col. 8, ll. 43-45. It is a preferred embodiment of the sector organization claimed in the claim 1 and 10 methods. In short, Ritek's argument is misplaced. The specification does not contradict the plain meaning of claims 1 and 10.

C.

The prosecution history does not compel a contrary result. The court must always consult the prosecution history, when offered in evidence, to determine if the inventor surrendered disputed claim coverage. *See Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 [74 USPQ2d 1184] (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history.").

After consulting the prosecution history, the trial court ruled that SanDisk disclaimed any

method or device in which Flash EEprom memory cells were not grouped into partitioned sectors. Ritek urges the court to affirm this analysis. SanDisk, however, maintains that the trial court erred in this conclusion. Instead, SanDisk argues, nothing in the prosecution history provides a clear and unmistakable disclaimer as found by the district court. On reviewing the relevant arguments to the examiner, we agree with SanDisk.

1.

When the patentee makes clear and unmistakable prosecution arguments limiting the meaning of a claim term in order to overcome a rejection, the courts limit the relevant claim term to exclude the disclaimed matter. *See Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 [67 USPQ2d 1321] (Fed. Cir. 2003) ("[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender."); *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 452 [227 USPQ 293] (Fed. Cir. 1985) ("[T]he prosecution history (or file wrapper) limits the interpretation of claims so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim allowance.").

As this court has explained,

> The doctrine of prosecution disclaimer [precludes] . . . patentees from recapturing through claim interpretation specific meanings disclaimed during prosecution. *See Schriber-Schroth Co. v. Cleveland Trust Co.*, 311 U.S. 211, 220-21 (1940) ("It is a rule of patent construction consistently observed that a claim in a patent as allowed must be read and interpreted with reference to claims that have been cancelled or rejected, and the claims allowed cannot by construction be read to cover what was thus eliminated from the patent."); *Crawford v. Heysinger*, 123 U.S. 589, 602-04 (1887); *Goodyear Dental Vulcanite Co. v. Davis*, 102 U.S. 222, 227 (1880); *cf. Graham v. John Deere Co.*, 383 U.S. 1, 33 [148 USPQ 459] (1966) (ruling, in addressing the invalidity of the patents in suit, that "claims that have been narrowed in order to obtain the issuance of a patent by distinguishing the prior art cannot be sustained to cover that which was previously by limitation eliminated from the patent").
>
> . . . .
>
> As a basic principle of claim interpretation, prosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution. *See Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1347 [47 USPQ2d 1418] (Fed. Cir. 1998).

Omega, 334 F.3d at 1323-24.

An ambiguous disclaimer, however, does not advance the patent's notice function or justify public reliance, and the court will not use it to limit a claim term's ordinary meaning. *See id.* at 1324 (collecting cases). There is no "clear and unmistakable" disclaimer if a prosecution argument is subject to more than one reasonable interpretation, one of which is consistent with a proffered meaning of the disputed term. *See Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 [69 USPQ2d 1481] (Fed. Cir. 2004) (finding no disclaimer because "the statements in the prosecution history are subject to multiple reasonable interpretations, they do not constitute a clear and unmistakable departure from the ordinary meaning of the term [at issue]"); *Cordis Corp. v. Medtronic AVE, Inc.*, 339 F.3d 1352, 1359 [67 USPQ2d 1876] (Fed. Cir. 2003) (concluding that a statement made during prosecution "is amenable to multiple reasonable interpretations and it therefore does not constitute a clear and unmistakable surrender"). The question, therefore, is whether any of SanDisk's prosecution arguments to the examiner have no reasonable interpretation other than to disavow any memory system in which Flash EEprom memory cells are not grouped into partitioned sectors.

2.

In this case the relevant prosecution argument responded to an obviousness rejection. The '987 patent issued from application Ser. No. 174,768 ("the '768 application"). On December 7, 1995, the examiner rejected original claims 79 (which issued as claim 1) and 85 (which issued as claim 10) in the '768 application as obvious under Burke in view of Yomoto. The examiner explained that Burke—an Australian patent, No. AU-B-22536/83—taught a memory system including

"an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to 'emulate' a magnetic disk which has sectors." As the examiner explained, Yorimoto—European patent application No. 86114972.2, Pub. No. 0 220 718—"teaches partitioning the cells with a sector into portions, each portion is for storing a specific type of information." Rejecting claim 85 (issued claim 10), the examiner concluded,

> It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Yorimoto's memory (of EEPROM type) and Yorimoto's memory cells partitioning in place of Burke's memory.
>
> The artisan would have been motivated to use Yorimoto's EEPROM in the place of Burke's memory because Yorimoto's EEPROM can be partitioned into sectors and Burke's emulation inherently suggests that the emulating memory should be able to emulate the sectors of Burke's magnetic disk.

SanDisk argued that the examiner was mistaken. In particular, SanDisk explained:

> The memory cell array is divided into sectors, with the cells within each sector being erasable together as a unit. Stored in each sector is a sectors [sic] worth of user data and some overhead information (a header) about the sector and/or about the user data stored in the sector.

(quoted at Pretec SJ Order, slip. op. at 25). Relying heavily on SanDisk's description of "*each* sector", the trial court concluded that SanDisk was referring to every sector on the 987 patent EEproms. *Id.* at 26. Ritek contends that the trial court's analysis was correct, and with this language SanDisk disclaimed its current claim construction. We disagree, and find no clear and unmistakable disclaimer in this passage.

[3] The trial court's and Ritek's reasoning assumes its conclusion. The quoted passage begins with the proviso that "The claims are directed to a flash EEPROM system[,]" If, when viewed in context, SanDisk used this passage to describe the memory cell array—and, in particular, the claimed sector organization subject to the methods in original claims 79 and 85—then there is no prior reason why that memory cell array or the discussion of it should be presumed to exhaust every cell on every EEprom in the "memory system" recited in the claim preambles. Given the open language in the claims, there is no reason for the court to read the prosecution argument with such a presumption in mind. Put differently, the reference to "each sector" means "each sector" subject to the claimed method, and no more. In short, SanDisk's reading of this prosecution argument is at least reasonable. Thus, focusing on this passage alone, there is no "clear and unmistakable surrender" within the meaning of *Golight*.

The trial court further reasoned that because SanDisk sought to emulate a disk drive with the claimed memory system, it followed that SanDisk intended to group every Flash EEprom memory cell into a partitioned sector. The trial court focused on the following prosecution argument, responding to the obviousness rejection of original claim 79:

> The claims in this application each define more than the desire to make a semiconductor memory system look on the host system side of the memory controller to be a disk drive. They define a way of configuring and using a semiconductor memory on the memory side of the controller in a way similar to a disk drive. Claim 79 defines a flash EEPROM system with an array that is divided into sectors of cells that are erasable together as a unit. This is not new by itself but is a particular type of memory . . . to be used to emulate a disk drive. None of the . . . cited references suggest use of such a type of memory. The only mention of an EEPROM system is by Yorimoto et al. but their embodiments appear to be generically described for use with either an EEPROM or a battery backed volatile RAM. Nothing is said by Yorimoto et al. of a flash EEPROM system that is operated with sectors of cells that are erasable together as a unit. It is the use of this type of memory that allows the memory itself to be operated very similarly to that of a disk drive, with individual sectors that store both user data and overhead data (a header for the sector). It is the operation of the flash EEPROM memory by the memory controller with the sectored and partitioned characteristics of a disk drive memory that is novel and non-obvious.

Ritek contends that the trial court correctly read this passage to disclaim the claim construction set forth above. Again, we disagree.

First, as with the last passage, this argument is directed to explicating the claimed invention. It does not purport to exclude from the "memory system" other configurations of Flash EEprom memory cells. Even though SanDisk identifies the novel invention as "operation of the flash EEPROM memory by the memory controller with the sectored and partitioned characteristics of a disk drive memory," that statement goes to the claimed memory organization.

Second, the fact that with the claimed invention SanDisk sought to emulate a disk drive memory storage configuration does not compel the conclusion that SanDisk required every Flash EEprom memory cell in the "memory system" recited in the claims to be grouped into partitioned sectors. The trial court's reasoning, in short, relies on a false analogy. Though every memory cell on a disk drive might have a physical location in a partitioned sector, it does not follow that to "emulate" that function every memory cell in a Flash EEprom array must also be so grouped. To the contrary, the organization of memory cells in the Flash EEprom is physically limited only by the requirement of a simultaneous erase by sector; in other respects, the cells are grouped into sectors by a logical allocation. Thus, while physical organization of memory on a disk drive might require every memory cell to be placed in a partitioned sector, the physical organization of memory cells on an EEprom does not.

The prosecution history as a whole confirms this point. In an earlier passage, SanDisk argued:

> The *claimed memory system* looks to the host computer as if it was a disk drive system, similar to the goal stated in the cited Burke patent. But a significant difference is the claimed operation *of the flash EEPROM array* with many incidents of a disk system. It is divided into sectors that are operated as a unit, including overhead data (a header) as well as user data, and, in some of the claims, the overhead data is read from an addressed sector before user data is written into that sector.

(emphases added). The passage focuses on the claimed operation of the flash EEprom memory cell array, the subject of claims 1 and 10; it does not address itself to unclaimed uses of the memory cells. Moreover, according to SanDisk, that particular EEprom configuration was not obvious from combining Burke, which emulated a disk drive, and Yorimoto, which claimed an EEprom array:

> This is quite different from the way that semiconductor memory arrays are usually operated. . . . The present claims . . . define a disk like approach to semiconductor memory operation. The fact that the system of the Burke patent may look to the host system as a disk memory system does not mean that its array is operated in sectors, with headers, etc., as claimed. . . .
>
> . . . [T]he flash EEPROM system employed in the present invention, unlike typical RAMs, do have memory operations that can benefit from auxiliary information. The provision for making such information available in a header of each sector in the context of a solid state memory is part of the present invention.
>
> An underlying assumption made throughout the Examiner's Action is that it is *inherent* in the system of the cited Burke reference to operate its volatile RAM array with sectors, and thus obvious to include overhead data (headers) in individual sectors. This premise, and thus all the rejections based upon it, is respectfully submitted to be incorrect. Contrary to the position taken in the Examiner's Action, it is submitted that the fact that Burke's system looks to the host system as a disk drive memory does not compel this conclusion. The alleged inherent Burke disclosure upon which nearly all the grounds of rejection are based does not exist.

In other words, it was novel to organize the cells into partitioned sectors for purposes of the claim, but the claimed purpose of emulating a disk drive did not compel sorting every memory cell—even those not subject to the claimed method—in that fashion.

In sum, we conclude that SanDisk did not unmistakably surrender the grouping of Flash EEprom memory cells into non-partitioned sectors. The prosecution history is consistent with the plain meaning of claims 1 and 10, and does not compel the trial court's contrary reading.

D.

Ritek argues that equity requires judicially estopping SanDisk from arguing the claim

construction discussed above because SanDisk argued, in earlier litigation and on preliminary injunction in this action, that claims 1 and 10 required every memory cell in the Flash EEprom memory to be grouped into partitioned sectors.[3] Thus, according to Ritek, "SanDisk should be estopped from playing fast and loose with the courts by changing the meaning of its patent claims simply because its interests have changed now that it knows how Ritek's products work." Ritek Br. at 25-26. We find this argument misplaced.

Judicial estoppel is an equitable doctrine that prevents a litigant from "perverting" the judicial process by, after urging and prevailing on a particular position in one litigation, urging a contrary position in a subsequent proceeding—or at a later phase of the same proceeding—against one who relied on the earlier position. *See Hamilton v. State Farm Fire & Cas. Co.*, 270 F.3d 778, 782 (9th Cir. 2001); *Data Gen. Corp. v. Johnson*, 78 F.3d 1556, 1565 (Fed. Cir. 1996). It is within the trial court's discretion to invoke judicial estoppel and preclude an argument. *Id.* Here, the trial court did not apply the doctrine and the appellees ask this court, in its appellate jurisdiction, to find an estoppel.

As the Supreme Court recently explained,

> Where a party assumes a certain position in a legal proceeding, and succeeds in maintaining that position, he may not thereafter, simply because his interests have changed, assume a contrary position, especially if it be to the prejudice of the party who has acquiesced in the position formerly taken by him.

New Hampshire v. Maine, 532 U.S. 742, 749 (2001) (cit. omitted); *see also id.* at 749-50 (collecting cases). In *New Hampshire*, the Supreme Court identified several factors guiding the decision to apply judicial estoppel: (1) the party's later position must be "clearly inconsistent" with the earlier position; (2) the party must have succeeded in persuading a court to adopt the earlier position in the earlier proceeding; and (3) the courts consider "whether the party seeking to assert an inconsistent position would derive an unfair advantage or impose an unfair detriment on the opposing party if not estopped." *Id.* at 751. These factors, while not exclusive, must guide the court's application of its equitable powers. *Id.*

[4] Ritek's judicial estoppel argument loses force when tested against these criteria. First, in the *Lexar* litigation, SanDisk never advanced a claim construction that was "clearly inconsistent" with the partitioning analysis discussed above. The trial court in *Lexar* therefore cannot be said to have adopted such a position at SanDisk's urging. The district court here recognized that very point in its summary judgment and claim construction order. As it noted, "SanDisk's argument [for the analysis set forth above] draws some strength from the limited nature of the *Lexar* court's construction. The *Lexar* court did not explicitly construe the broader phrase from the patent [citing partitioning step]. The *Lexar* court limited its construction to the 'user data and overhead data portions' of claims 1 and 10." As SanDisk observes, the issue before Judge Breyer in *Lexar* was whether the sectors subject to the claim 1 and claim 10 methods were limited to a *single* user and data portion, or whether those sectors could be further partitioned. In short, *Lexar* involved a different dispute concerning the claim terms.

Second, SanDisk's arguments at preliminary injunction in this action were no more "clearly inconsistent" than the arguments in *Lexar*. In support of preliminary injunction, SanDisk argued that the preamble to claims 1 and 10 required "partitioning the array of non-volatile memory sector cells into at least a user data region and an overhead data region." SanDisk further argued, invoking the *Lexar* construction of "partitioned", that the claim required "each non-volatile memory sector must have at least one user data portion and one overhead data portion, but is not limited to only one data user portion and only one overhead data portion."

As explained above, these arguments are directed to the claimed method, and the claims do not preclude additional memory cells that are not organized according to that method. Moreover, at preliminary injunction SanDisk plainly urged the *Lexar* claim construction, and that analysis did not extend to the issue at bar. Thus, there was no inconsistency between the arguments at preliminary injunction, and the disputed construction now on appeal. In sum, the factual premise of Ritek's argument

[3] Pretec adopted Ritek's arguments by reference. Memorex filed a joinder in Pretec's brief. Each appellee thus relies on Ritek's judicial estoppel argument.

is misplaced. There is no basis for judicial estoppel here.

Moreover, the equities do not favor applying judicial estoppel to prevent claim construction arguments from evolving after preliminary injunction. The law provides, for example, that the trial court is free to revisit an initial claim construction adopted for preliminary injunction, recognizing that a preliminary construction made without full development of the record or issues should be open to revision. *See Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1375 [74 USPQ2d 1586] (Fed. Cir. 2005). After discovery the court expects the parties to refine the disputed issues and learn more about the claim terms and technology, at which point a more accurate claim construction can be attempted. That is precisely what happened here. If, as it appears, SanDisk initially thought every memory cell on the accused Ritek products came within the claimed method, then there was no occasion to consider whether other, non-sectored or non-partitioned sectors of memory cells could be used in conjunction with claims 1 or 10. Thus, the present dispute only became an issue after further discovery. Applying judicial estoppel here would subvert the useful function of pre-trial discovery and motion practice in focusing issues for trial. In sum, judicial estoppel does not prevent SanDisk from maintaining its current claim construction arguments.

E.

The parties further dispute the meaning of "array" as used in claims 1 and 10. The trial court determined that "array" meant a collection of Flash EEprom memory cells on one or more EEprom chips. SanDisk argues, to the contrary, that by the plain meaning expressed in technical dictionaries "array" refers only to a collection of cells on a single integrated circuit or chip. Ritek argues that the '987 patent uses array in a specific sense, at odds with the plain meaning, but consistent with the trial court's interpretation. Ritek further argues that judicial estoppel applies, with special force, to the proper reading of "array".

As noted above, the difference does not alter the trial court's judgment of no infringement. The judgment does not depend on the choice between these disputed meanings of "array". It turns, instead, on the district court's reading of the partitioning requirements in the claims. Because this court reviews judgments rather than claim construction orders, we find it unnecessary at this point to decide this dispute.

III.

[5] Pretec urges the court to affirm the judgment of no infringement in view of its arguments concerning the meaning of "corresponds" in claims 1 and 10. Pretec made the same claim construction and infringement arguments to the trial court after the relevant cut-off dates under the Northern District's Patent Local Rules and the trial court's scheduling order. The district court refused to entertain Pretec's untimely arguments. As explained in *Genentech, Inc. v. Amgen, Inc.*, 289 F.3d 761, 774 [62 USPQ2d 1640] (Fed. Cir. 2002), this court gives broad deference to the trial court's application of local procedural rules in view of the trial court's need to control the parties and flow of litigation before it. "[T]his court defers to the district court when interpreting and enforcing local rules so as not to frustrate local attempts to manage patent cases according to prescribed guidelines." *Id.* The district court's application of the local rules are within its sound discretion, and when reviewing that exercise of discretion "this court determines whether (1) the decision was clearly unreasonable, arbitrary, or fanciful; (2) the decision was based on an erroneous conclusion of law; (3) the court's findings were clearly erroneous; or (4) the record contains no evidence upon which the court rationally could have based its decision." *Id.* None of these criteria for setting aside the district court's ruling are satisfied here. In sum, Pretec shows no abuse of discretion in the district court's ruling, and indeed we discern none.[4]

IV.

The district court erred in its claim construction. The limiting preambles in claims 1 and 10 are written in open language, and the claims are not limited to memory systems in which every memory cell is grouped into a partitioned sector. The judgment of no infringement rests on an erroneous claim construction, and the court vacates it. The case is remanded for further proceedings.

[4] We do not decide whether, at trial on the merits, Pretec can or should be precluded from presenting these claim construction and non-infringement arguments.

VACATED AND REMANDED

Each side shall bear its own costs.

Benson v. Ginter

U.S. Patent and Trademark Office
Board of Patent Appeals and Interferences

Interference No. 105,142

Decided November 17, 2004

(Nonprecedential)

PATENTS

[1] Practice and procedure in Patent and Trademark Office — Prosecution — Duty of candor — Materiality (§ 110.0903.04)

Practice and procedure in Patent and Trademark Office — Interference — Burden of proof (§ 110.1707)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Party filing preliminary motion in interference has burden of establishing that it is entitled to relief requested, which, for motion alleging inequitable conduct due to failure to disclose material information, requires at least threshold level of materiality of undisclosed reference, and threshold level of intent to mislead or deceive U.S. Patent and Trademark Office; in present case, senior party's motion alleging that junior party violated duty of disclosure must be dismissed without consideration of junior party's opposition or senior party's reply, since senior party's exhibit purporting to illustrate allegation of inequitable conduct merely shows drawing of invention described in interference counts, and does not indicate closest known prior art, since senior party has not established that text document to which senior party refers in its allegations was written by individual subject to duty of disclosure, and since, even if author of document was under such duty, senior party's motion paper does not give rise to inference of threshold level of intent to mislead or deceive PTO, and senior party's counsel declined prior opportunity to request taking of testimony in support of its motion.

[2] Practice and procedure in Patent and Trademark Office — Prosecution — Filing date (§ 110.0906)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Preliminary motion of junior party in interference seeking to be accorded benefit of filing date of foreign application is granted, since senior party did not file opposition, and since motion sets forth prima facie case of entitlement to relief requested.

[3] Practice and procedure in Patent and Trademark Office — Interference — Counts (§ 110.1703)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Preliminary motion of junior party in interference seeking to redefine interference by substituting proposed count for existing count is granted, even though junior party perfected its claim of priority to foreign application in order to overcome rejection of claims including those corresponding to existing count, since reasonable conclusion is that examiner recommending interference was asserting that claims were allowable after junior party overcame rejection, since patentability of subject matter of proposed new count is not at issue, since testimony of junior party's expert, who concluded that relevant language in existing count is essentially same as corresponding portion of proposed count, will be accorded some weight, in that language in counts is similar and expert is entitled to give opinion based on prior professional and technical experience, and since scope of proposed count, as whole, is clearly different from that of existing count, and junior party does not suggest otherwise.

[4] Practice and procedure in Patent and Trademark Office — Prosecution — Disclaimer (§ 110.0925)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Preliminary motions of junior party in interference, alleging that senior party's involved claims are unpatentable for obviousness-type double patenting, are considered withdrawn, since senior party filed terminal disclaimers to obviate charges of double patenting.